INVESTIGATION AND PREDICTION OF SOLDER JOINT RELIABILITY FOR CERAMIC AREA ARRAY PACKAGES UNDER THERMAL CYCLING, POWER CYCLING, AND VIBRATION ENVIRONMENTS

A Dissertation
Presented to
The Academic Faculty

by

Andrew Eugene Perkins

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of G.W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
May 2007

INVESTIGATION AND PREDICTION OF SOLDER JOINT RELIABILITY FOR CERAMIC AREA ARRAY PACKAGES UNDER THERMAL CYCLING, POWER CYCLING, AND VIBRATION ENVIRONMENTS

Approved by:

Prof. Suresh K. Sitaraman, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Prof. Daniel Baldwin
School of Mechanical Engineering
Georgia Institute of Technology

Prof. Rao Tummala
School of Electrical and Computer Engineering & School of Materials Science and Engineering
Georgia Institute of Technology

Prof. Richard W. Neu
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Kamal Sikka
Thermal/Mechanical Design
IBM Microelectronics

Date Approved: March 27, 2007

Dedicated to my Grandfather William Dana Perkins.

He taught me that everything holds a mystery. The pursuit of that mystery leads to knowledge, and that knowledge leads again to mystery. This infinite circle is his joy and pursuit-contagious to all those around him. I feel his joy now as I complete this body of knowledge and enter into another mystery.

ACKNOWLEDGEMENTS

I began this PhD thinking *I* was going to attain all the necessary knowledge and skills to complete a PhD. However, I soon realized that pursing a PhD is not worthwhile, nor an achievable goal to pursue by oneself. I have been blessed with many supporters along the way. Without them I would never have finished this work.

I would first like to acknowledge my advisor, Dr. Sitaraman, for taking me in as an undergraduate student and giving me an open door to working with him as a graduate student. I appreciate his honesty, encouragement when I was off-track, and willingness to put forward the necessary effort and endurance to help me complete this work.

In addition to Dr. Sitaraman, I would like to thank the other members of my PhD Reading Committee: Dr. Tummala, Dr. Baldwin, Dr. Neu, and Dr. Sikka. They provided valuable input, generous use of their lab equipment, and helpful feedback during the process.

I would like to thank the following companies: Compaq/HP for initiating the project, funding, and provided test vehicles; the Package Research Center of Georgia Tech for use of equipment and helpful daily interaction; Northrop Grumman and BAE Systems for providing environmental condition data and funding; IBM Microsystems for a valuable summer internship and support of this work; and Micron Technologies for allowing me to finish this work while working full-time as an employee.

I would like to thank my wife, Lynn, for her support and giving me many reasons to have enjoyed this journey as deeply as I have. The cyclical nature of a graduate student's life and emotions is often more harsh on the supporting partner. I can't think of a greater blessing than to have had her support and willingness to sacrifice so much for this work.

I would like to thank my parents giving me so many open doors in life. They have encouraged me along the way and now they get to reap the benefits of their work in me as Lynn and I strive to raise their grandsons with the same encouragement they gave to me.

I would also like to thank my innumerable friends and family members who have made life worth living. One cannot grow in life without the love of others.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS……iv

LIST OF TABLES……..ix

LIST OF FIGURES……....xi

LIST OF ABBREVIATIONS……...xvi

LIST OF SYMBOLS…….……....xvii

SUMMARY ……..…xix

CHAPTER 1. INTRODUCTION 1

CHAPTER 2. LITERATURE REVIEW 5
2.1. Thermal Cycling 5
2.2. Power Cycling.....8
2.3. Vibration Environment 13
2.4. Combined and Sequential Thermal-Mechanical, Power Cycling, and Vibration Environments 15

CHAPTER 3. RESEARCH GAPS, RESEARCH OUTLINES, AND THESIS OUTLINE….. 17
3.1. Research Gaps in Existing Body of Literature 17
3.2. Research Objectives.....18
3.3. Thesis Outline 20

CHAPTER 4. BACKGROUND 22
4.1. CCGA and CBGA Electronic Packages 22
4.2. CCGA Test Vehicle Description 25
4.3. Solder Material Behavior and Fatigue 26
4.4. Cumulative Damage Prediction: Miner's Rule.....37
4.5. Laser Moire Interferometry.....39
4.6. Vibration Theory.....42
4.7. Chapter Summary 52

CHAPTER 5. UNIFIED FINITE ELEMENT MODELING METHODOLOGY FOR PREDICTION OF SOLDER JOINT RELIABILITY UNDER THERMAL, POWER, AND VIBRATION ENVIRONMENTS FOR CERAMIC AREA ARRAY ELECTRONIC PACKAGES.....53
5.1. Introduction.....53
5.2. Unified Finite Element Modeling methodology 53
5.3. Chapter Summary 70

CHAPTER 6. VALIDATION OF UNIFIED FEM FOR THERMAL CYCLING AND POWER CYCLING ENVIRONMENTS 72
6.1. Introduction....72
6.2. Laser Moire Interferometry....72
6.3. Accelerated Thermal Cycling Verification with Laser Moire Interferometry...88
6.4. Importance of including creep in every solder joint of FEM....91
6.5. Power Cycling PC Verification 92
6.6. Chapter Summary 94

CHAPTER 7. PREDICTIVE FATIGUE LIFE UNDER THERMAL CYCLING AND POWER CYCLING ENVIRONMENTS 95
7.1. Introduction....95
7.2. CBGA: 63Sn37Pb solder joint fatige life 95
7.3. CCGA: 90Pb10Sn solder Joint fatige life....101
7.4. Chapter Summary 105

CHAPTER 8. VALIDATION OF UNIFIED FEM AND DEVELOPMENT OF FATIGUE LIFE MODEL FOR VIBRATION....106
8.1. Vibration Experimental Setup and Results....106
8.2. FEM Modal Analysis and Stress Distribution. 110
8.3. Dye-and-Pry Analysis of Test Vehicle D: Solder Joint Failure Location 112
8.4. Solder Joint Failure Mechanism and Microstructural Analysis....115
8.5. Fatigue Life Prediction for 90Pb10Sn Solder Under Vibration Loading 118
8.6. Validation of Predictive Models....123
8.7. Discussion on Validation....128
8.8. Chapter Summary 128

CHAPTER 9. DEVELOPMENT OF UNIVERSAL PREDICTIVE FATIGUE LIFE EQUATION AND STUDY OF THE EFFECT OF DESIGN PARAMETERS 130
9.1. Introduction....130
9.2. Method....131
9.3. Discussion of the Predictor Variables....142
9.4. Verification of Predictive Equation Using Literature Data 147
9.5. Application: Military obsolescence and maintanence scheduling....149
9.6. Conclusions....152

CHAPTER 10. ACCELERATION FACTOR TO RELATE THERMAL CYCLES TO POWER CYCLES FOR CERAMIC BALL GRID AREA ARRAY PACKAGES....154
10.1. Introduction....154
10.2. Power Cycling Thermal Environment 154
10.3. Ceramic Ball Grid Array (CBGA)....156
10.4. Method to develop Acceleration Factor for relating ATC to PC....157
10.5. Application of developed AF Equation 163
10.6. Conclusions....167

CHAPTER 11. INVESTIGATION OF SOLDER JOINT FATIGUE FAILURE UNDER SEQUENTIAL THERMAL AND VIBRATION ENVIRONMENTS 169
11.1. Introduction.....169
11.2. Sequence Tests.....170
11.3. Nonlinear Cumulative Damage Rule.....171
11.4. Distribution of the Nonlinear Cumulative damage Index.....173
11.5. Extension of nonlinear sequential cumulative damage rule to include power cycling (PC).....175
11.6. Conclusions.....175

CHAPTER 12. RESEACH CONTRIBUTIONS AND FUTURE WORK 177
12.1. Research Contributions.....177
12.2. Future Work.....179

LIST OF TABLES

Table 4-1. Comparison of CBGA and CCGA 23

Table 4-2. I/Os available for substrate size and pitch 24

Table 4-3. Effect of Interconnect Stiffness and Heat Sink Mass on Fundamental Frequency 51

Table 5-1. Linear temperature independent material properties 63

Table 5-2. Plasticity and Creep data for 63Sn37Pb and 90Pb10Sn solder 64

Table 5-3. Compatibility for Element types and Material Models for solder 67

Table 5-4. CCGA Damage results from 3rd cycle. 70

Table 6-1. Comparison of experimental to FEM predicted temperatures. 93

Table 6-2. Validation of power cycling FEM for CBGA 94

Table 7-1. CBGA experimental data from literature used to develop predictive equation for ATC and PC 96

Table 7-2. Developed Coffin-Manson and crack growth equations 99

Table 7-3. CBGA experimental data from literature used to validate predictive equation for ATC 101

Table 7-4. Results of CCGA ATC fatigue life tests. 102

Table 7-5. CCGA experimental data from literature used to develop predictive equation for ATC and PC 103

Table 7-6. CCGA experimental data from literature used to validate predictive equation for ATC and PC. 105

Table 8-1. Results for sinusoidal vibration testing of G_{in} =1G at f_n 109

Table 8-2. Fundamental Frequency of FR4 with 1089 I/O Component 111

Table 9-1. Steps to derive the universal predictive fatigue life equation 132

Table 9-2. Design of simulation (DOS) and predicted N_{50} for CBGA under ATC 133

Table 9-3. Results of linear regression analysis 136

Table 9-4. Values of Type A and B standard uncertainties. 141

Table 9-5. Comparison of Substrate Size and Number of Solder Joints 143

Table 9-6. Material Properties for Ceramic Substrate 144

Table 9-7. Proportional Changes in CBGA Solder Balls, Pads, and Solder Paste Volume with Solder Joint Pitch [126]. 145

Table 9-8. Literature cases used to assess validity of the predictive equation 148

Table 10-1 Effect of PWB normal thermal conductivity.....156

Table 10-2. Final Fatigue Predictive Equations for ATC and PC 162

Table 10-3. Test Cases for AF relating PC to ATC.....163

Table 10-4 Comparison of high and low substrate thermal conductivity. 163

Table 10-5. Alumina and HICTE substrate comparison.....165

Table 10-6. Number of ATC cycles to qualify a package (case 3) for a given desktop field life. 166

Table 11-1. Results of Sequential T-V and V-T tests. 171

Table 11-2. Comparison of linear and nonlinear *CDI* distributions 174

LIST OF FIGURES

Figure 1-1. (a) Rent's Rule [1] (b) Evolution of Packaging Technology [2] 1

Figure 3-1. Unified Modeling Methodology 20

Figure 4-1. Cross-section of a Ceramic Column Grid Array (CCGA). 23

Figure 4-2. Cross-section of a CBGA with 0.89mm diameter 90Pb10Sn ball [75]. 23

Figure 4-3. CCGA test vehicle on 137mm x 56mm x 2.8mm FR4 board.....25

Figure 4-4. Electrically monitored daisy chain rings of CCGA 26

Figure 4-5. Rheological model representing solder behavior. 27

Figure 4-6. Stress-strain response for simple rheological model of solder to a stress step load.....27

Figure 4-7. (a) Perfectly Plastic. (b) Elastic linear hardening. (c) Nonlinear Hardening.28

Figure 4-8. Stress-strain curve temperature dependence for (a) 60Sn40Pb and (b) 90Pb10Sn solders .[77] 29

Figure 4-9. Reverse yielding showing multilinear kinematic hardening (MKIN) and multilinear isotropic hardening (MISO) 29

Figure 4-10. Primary, secondary, and tertiary stages of creep strain under a constant load. [78].....30

Figure 4-11. Climb of an edge dislocation permitting glide to continue. [78] 31

Figure 4-12. Typical accelerated thermal cycle (ATC) 33

Figure 4-13. (a) Shakedown stabilization of stress-strain hysterisis, (b) ratcheting of stress-strain hysterisis loop due to mean stress effects. 33

Figure 4-14. Stress-Strain hysterisis loop for CBGA under 0/10oC 2cph ATC.....34

Figure 4-15. Stabilized stress-strain hysterisis loop showing common damage parameters. 35

Figure 4-16. Schematic of four beam moire interferometry to produce deformation fringes Nx and Ny. [105] 39

Figure 4-17. Schematic illustration of the deformation of the CBGA package assembly during the thermal cycle [108] 41

Figure 4-18. Schematic illustration of the deformation mechanism of a CCGA column during thermal cycling [107]. 42

Figure 4-19. SDOF system under harmonic excitation. 43

Figure 4-20. Nondimensional amplitude Eq. (4.24) and phase angle Eq. (4.25) for a harmonic SDOF.[109] 45

Figure 4-21. Schematic for analytical model of CCGA on FR4 board 47

Figure 4-22. Mode Shapes from analytical method for FR4 with a 1089 I/O CCGA. 50

Figure 4-23. Effect of Stiffness on First Mode Shape 51

Figure 5-1. 3D quarter FEM with solid detailed joint and equivalent beam for CCGA 56

Figure 5-2. 3D quarter FEM with solid detailed joint and equivalent beams for CBGA 56

Figure 5-3. Equivalent Beam Model for 1.27mm pitch CCGA 58

Figure 5-4. Equivalent Beam Model for 1.27mm pitch CBGA 59

Figure 5-5. 3D quarter FEM of CCGA with boundary conditions 61

Figure 5-6. Full FEM of CCGA under vibration loading with constrained boundary conditions 63

Figure 5-7. Hysterisis loops for CCGA with 20°C as stress-free temperature. 69

Figure 5-8. Hysterisis loops for CCGA with 183°C as stress-free temperature. 69

Figure 6-1. Schematic of the PEMI II moire setup for observing real-time deformations during thermal cycling. [108] 73

Figure 6-2. Cross-section of prepared sample before grating application 74

Figure 6-3. Temperature profile for laser moire interferometry of CCGA 75

Figure 6-4.Whole-field displacement V field (left) and U field (right). Only the left half of the sample is shown. 76

Figure 6-5. Vertical displacement of the ceramic substrate for CCGA 77

Figure 6-6. Relative horizontal displacement between ceramic substrate and board across the height of the solder joints for CCGA. 78

Figure 6-7. *U* and *V* displacement fields of the outermost CCGA solder joint 79

Figure 6-8. Effect of lid shown to minimize bending. 80

Figure 6-9. CCGA with no lid shows package bending. 81

Figure 6-10. Temperature profile for laser moire interferometry of CBGA....82

Figure 6-11. Whole-field displacement moire fringes for CBGA 83

Figure 6-12. Ceramic substrate vertical displacement at outermost solder joint number 12 for CBGA....84

Figure 6-13. Relative horizontal displacement between ceramic substrate and board across the height of the solder joints for CBGA. 86

Figure 6-14 *U* and *V* displacement fields of the outermost CBGA solder joint 87

Figure 6-15. *U* displacement fringes at -55°C showing high strain gradients in 63Sn37Pb fillet....87

Figure 6-16. *U* and *V* whole-field displacement of FEM (a,b) and Laser Moire (c,d) at 100°C for CCGA 88

Figure 6-17. *U* and *V* displacements of outermost solder joint at 100°C for FEM (a,b) and Laser Moire (c,d). for CCGA....89

Figure 6-18. *U* and *V* whole-field displacement of FEM (a,b) and Laser Moire (c,d) at -55°C for CBGA 90

Figure 6-19. *U* and *V* displacements of outermost solder joint at -55°C for FEM (a,b) and Laser Moire (c,d). for CBGA....90

Figure 6-20. Effect of Modeling Creep in Equivalent Beams 91

Figure 6-21. Temperature distribution of FEM used to valid PC FEM....93

Figure 7-1. Test box for ATC tests. 101

Figure 7-2. Total strain range strain vs fatigue life....104

Figure 8-1. Experimental setup for CCGA on FR4 board with clamped edges. 107

Figure 8-2. Linear sweep test for test vehicle A to determine the damping ratio ξ. 108

Figure 8-3. G_{out} versus fatigue life cycles for Ring 0, Ring 1, and Ring XX. 110

Figure 8-4. FEM mode shapes of 1089 CCGA Package on FR4 Board.....111

Figure 8-5. Axial stress distribution of CCGA solder columns under vibration 112

Figure 8-6. Special removal fixture to remove substrate from board for dye-n-pry analysis.....113

Figure 8-7. Dye and pry analysis of showing crack growth and distribution 114

Figure 8-8. Ductile cup/cone failure of solder joints due to substrate removal vs. brittle failure due to vibration fatigue.....115

Figure 8-9. Fatigue of CCGA column under: (a) vibration loading. Note column is not distorted and no necking. (b,c) thermal cycling. Observe deformation and necking of 90PB10Sn column at 63Sn37Pb fillet.....116

Figure 8-10. Cross-section scanning electron microscopy images of (a) virgin sample, (b) vibration failure, and (c) ATC failure 116

Figure 8-11. SEM images of high cycle fatigue crack in 90Pb10Sn column. 118

Figure 8-12. Weibull Fit of Fatigue data for 1.0G at natural frequency 119

Figure 8-13. Vonmises stresses for J_0 solder joint under a 1G sinusoidal acceleration driven at the f_n of 308Hz. 122

Figure 8-14. Plot of N_{50_exp} versus σ_a for each daisy chain ring. 122

Figure 8-15. Normalized Fatigue Life for CCGA solder joint array based on input acceleration G_{in} of 1G 124

Figure 8-16. Increments for predicting fatigue life by Miner's Rule 127

Figure 9-1. (a) Normal Probability Plot (b)Main Effects (c) Interaction Effects 136

Figure 9-2. Simple Analysis Tool for Avionics Maintenance. Example A 150

Figure 9-3. Complex Analysis Tool for Avionics Maintenance. Example B 151

Figure 9-4. Periodic maintenance tool: Example C 151

Figure 10-1. 1D Thermal Resistor Network for CBGA 155

Figure 10-2. Temperature gradients for (a) Case 1, k_{sub} = 0.002 W/mm K, and (b) Case 2, k_{sub} = 0.021 W/mm K.....164

Figure 10-3. Design based AF for several common ATC and PC environments at 50% failure. 167

Figure 11-1. Plot of n_1/N_1 vs n_2/N_2 for sequential loadings T-V (thermal followed by vibration) and V-T (vibration followed by thermal) along with linear and nonlinear damage models.....173

LIST OF ABBREVIATIONS

AF	Acceleration factor
ANOVA	Analysis of Variance
ATC	Accelerated thermal cycle
CBGA	Cermaic ball grid array
CCGA	Cermaic column grid array
CDI	Cumulative Damage Index
CM	Coffin-manson
cph	Cycles per hour
CTE	Coeffecient of Thermal Expansion
DOS	Desing of simulation
FEM	Finite Element Analysis
HICTE	High coeffecient of thermal expansion
MKIN	Multilinear Kinematic Hardening
MISO	Multilinear Isotropic Hardening
MSE	Error mean square
PC	Power cycling
ppm	Parts per million
PWB	Printed wiring board
SSE	Sum of Residual Errors

LIST OF SYMBOLS

α	Coefficient of thermal expansion
α_W	Characteristic fatigue life, 63.2% failure
β	Weibull Slope Paramter
$\Delta\varepsilon$	Strain range per cycle
ΔT	Temperature range
ΔW	Strain Energy density range per cycle
σ	Stress or Standard Deviation
σ_a	Stress amplitude per cycle
σ_y	Axial stress
ω	frequency of driving force, rad/s
Ψ	Damage Parameter
c	damping constant
ε	Strain
a	Crack size
f	Frequency in cycles per hour
f_n	Natural frequency, Hz
$F\%$	Percent failure of the population
k	Spring stiffness
m	Mass
N_{50}	Fatigue life cycles for 50% of components to fail

n_{DOF}	Number of degrees of freedom
n_{joints}	Number of solder joints
p	Level of confidence
Pb	Lead
Q_{DIE}	Heat from Die
R	Resistance
Sn	Tin
T	Kinetic energy
T_{peak}	Peak temperature of cycle
T-V	Thermal-Vibration
u	standard uncertainty
U	Horizontal displacements
V	Vertical displacements or Potential Energy
V-T	Vibration-Thermal

SUMMARY

Microelectronic systems are subjected to thermal cycling, power cycling, and vibration environments in various applications. These environments, whether applied sequentially or simultaneously, affect the solder joint reliability. Literature is scarce on predicting solder joint fatigue failure under such multiple loading environments. This thesis aims to develop a unified modeling methodology to study the reliability of electronic packages subjected to thermal cycling, power cycling, and vibration loading conditions. Such a modeling methodology is comprised of an enriched material model to accommodate time-, temperature-, and direction-dependent behavior of various materials in the assembly, and at the same time, will have a geometry model that can accommodate thermal- and power-cycling induced low-cycle fatigue damage mechanism as well as vibration-induced high-cycle fatigue damage mechanism. The developed modeling methodology is applied to study the reliability characteristics of ceramic area array electronic packages with lead-based solder interconnections. In particular, this thesis aims to study the reliability of such solder interconnections under thermal, power, and vibration conditions individually, and validate the model against these conditions using appropriate experimental data either from in-house experiments or existing literature. Once validated, this thesis also aims to perform a design of simulations study to understand the effect of various materials, geometry, and thermal parameters on solder joint reliability of ceramic ball grid array and ceramic column grid array packages, and use such a study to develop universal polynomial predictive equations for solder joint reliability. The thesis also aims to employ the unified modeling methodology to develop new understanding of the acceleration factor relationship between power cycling and thermal cycling. Finally, this thesis plans to use the unified modeling methodology to study solder joint reliability under the sequential application of thermal cycling and

vibration loading conditions, and to validate the modeling results with first-of-its-kind experimental data. A nonlinear cumulative damage law is developed to account for the nonlinearity and effect of sequence loading under thermal cycling, power cycling, and vibration loading.

CHAPTER 1

INTRODUCTION

An electronic package is designed to protect an Integrated Circuit (IC) from electrical, mechanical, chemical, and thermal harm while providing interconnections to other devices. This function becomes increasingly difficult as ICs become increasingly more complex in order to meet the self fulfilling prophecy of Moore's Law [1] which states that the transistor density on an IC will double every 18 months [2]. As an example, in 1971 Intel's 4004 chip had 2,250 transistors while in 2003 the Intel Itanium 2 Processor had 410 million transistors. The increase in transistor density relates to an increase in the number of interconnections coming from the chip. Rent's Rule [3], shown in Figure 1-1 is a power law equation commonly used as a predictor of the number of interconnects that will be needed as a function of the number of transistors. Electronic packaging technology has had to evolve as the complexity of the IC grew and required greater demands for electrical, mechanical, chemical, and thermal performance of the package. Figure 1 shows how packaging technology has evolved from the Dual Inline Package (DIP) to the chip scale packages (CSP) and ball grid array (BGA) solutions of today.

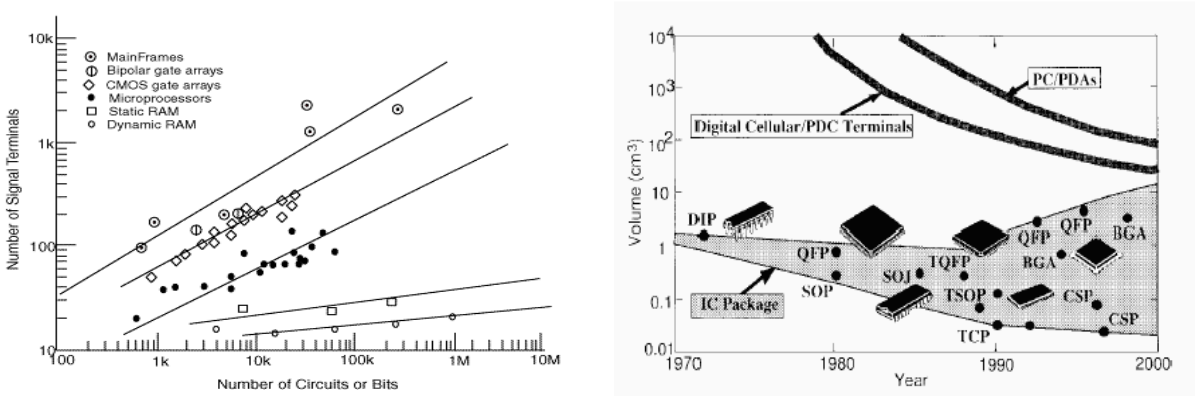


Figure 1-1. (a) Rent's Rule [1] (b) Evolution of Packaging Technology [2]

Solder joint reliability at both the first level (chip to substrate) and second level (substrate to PWB) of packaging is a driving concern for area array packages. For plastic packages, the first level packaging is of interest as the Coefficient of Thermal Expansion (CTE) mismatch between the chip and substrate is high, while that of the substrate to PWB is low. This work will focus on ceramic substrate packages such as Ceramic Column Grid Array (CCGA) and Ceramic Ball Gird Array (CBGA) where the second level of packaging is of greater concern due to the high CTE mismatch between the substrate and printed wiring board (PWB) [6]. In ceramic packages, the first level packaging is reliable for encapsulated wire-bonds or underfilled flip chips due to the low CTE mismatch between the chip and ceramic substrate [7]

Area array electronic packages are increasing in substrate size, having greater interconnect density, and becoming more complex in geometry and material properties[8]. These factors make it increasingly difficult to develop predictive equations for solder joint reliability. A typical approach to assessing solder joint fatigue reliability involves using analytical equations and numerical finite element models (FEM) for initial design, and experiments to confirm the failure modes and reliability of the electronic package. Analytical models are generally quick and easy-to-use, however, they are not able to capture complex geometric and material behavior effectively. Numerical models can capture complex geometric and material behavior, however, they require expertise in numerical modeling, material characterization, can be time-consuming, and require validation through experiments. In addition, the present numerical modeling techniques are not computationally efficient for electronic packages with greater than 1000 interconnects. Experimental tests are necessary for qualification of electronic packages and validating analytical/numerical models, however they are impractical for early design decisions because of high cost and lengthy test time. A combination of analytical, numerical, and experimental tests is necessary to develop solder joint fatigue predictive equations.

Electronic packages are subjected to a variety of harmful conditions/environments, three of which are considered in this thesis: (1) thermal cycling of the environment, (2) power cycling of the die(chip), and (3) vibration loading of the PWB. Other harmful conditions/environments such as moisture absorption and electromigration are not considered in this thesis.

Thermal cycling refers to situations where the environment surrounding the electronic package undergoes cyclic thermal excursions. Generally, the cycle consists of a dwell at a high temperature, a ramp to a low temperature, a dwell at the low temperature, a ramp to the high temperature, and the cycle is then repeated. The electronic package experiences an isothermal temperature as it comes to equilibrium with the environment during the high and low dwells. The CTE mismatch between the substrate and PWB causes the solder joints to deform and fatigue over many cycles Two common thermal cycling environments are the heating and cooling that occurs during a typical day during the morning and evening hours, and the heating and cooling of an automobile engine compartment upon a persons commute to and from their place of work.

Power cycling refers to situations where the heat source is the electronic package itself or a component of the package. For example, every electronic package has a chip that is powered and thus dissipates heat through joule heating. The chip acts as a heat source and temperature gradients develop in the package causing expansion of the substrate and PWB. The 2003 ITRS roadmap [9] shows chip power consumption for high performance chips increasing from 0.48 Watts/mm^2 in 2003 to 1.55 W/mm^2 in 2010 while the chip size stays at 310 mm2. This translates into a significant 3x increase of power consumption from 150 Watts in 2003 to 480 Watts in 2010. At the same time, the 2003 ITRS shows the maximum junction temperature for high performance chips dropping from 90^0C to 85^0C. The need for determining reliability under power cycling is critical along with the need for better thermal management solutions.

The low-cycle fatigue failure of lead tin eutectic solder joints due to the CTE mismatch is fairly well understood in literature [10, 11]. However, the literature available on high cycle vibration fatigue of solder joints is limited [12], partly due to the complexity of the problem. With large area array components such as a CCGA package, it is important to understand how the component may affect the vibration characteristics of the system and the solder joint fatigue life [10, 13]. This involves experimentally finding the natural frequencies, determining mode shapes, and observing failure of solder joints. Analytical and numerical models must be able to reproduce the essential vibration characteristics and incorporate solder joint behavior. The need for understanding vibration induced solder joint fatigue failure is especially important in harsh military environments [14].

Thermal cycling, power cycling, and vibration loading can also occur sequentially or simultaneously. Assessing solder joint reliability under the combined environments is difficult and typically only done for harsh environments such as military, space, or automotive environments.

In addition to assuring solder joint reliability under the environments mentioned above, it would also be helpful to develop easy-to-use, physics-based, and experimentally validated analytical equations to predict the reliability of solder joints. The majority of predictive equations that have been developed in the current literature are not general enough to be used by other researchers and persons without extensive mechanics and finite-element background, thus each researcher must develop their own equations. The electronic packaging community is performing costly redundant research due to the lack of universal fatigue equations for particular packages. There is a need to develop accurate, easy-to-use tools that can be used by persons without extensive mechanics and finite-element background to predict solder joint fatigue failure in electronic packages under thermal-mechanical, power cycling, and vibration environments.

CHAPTER 2

LITERATURE REVIEW

A literature review of experimental, analytical, and numerical work for area array packages under thermal cycling, power cycling, and vibration loading is presented in this chapter.

2.1. THERMAL CYCLING

The literature on thermal cycling of electronic components containing lead tin eutectic solder is abundant as accelerated thermal cycling (ATC) testing is one of the most common ways to test solder joint reliability.

2.1.1. Analytical Modeling

Analytical modeling of thermal-mechanical environments has been studied extensively in literature. The simplest and most prevalent equation, shown in Equation (2.1), also serves to highlight the most common cause of solder joint fatigue failure; the global CTE mismatch between the substrate and PWB causes the solder joint to fatigue as it must accommodate the difference in expansion between the substrate and PWB.

$$\gamma = \frac{L}{2h}\left(\alpha_{PWB}\Delta T_{PWB} - \alpha_{SUB}\Delta T_{SUB}\right) \tag{2.1}$$

where: γ is the engineering shear strain, L is the distance from the neutral point (DNP), h is the height of the solder joint, α is the Coefficient of Thermal Expansion (CTE), and ΔT is the temperature difference between the maximum and minimum temperature

For ATC tests, $\Delta T_{SUB} = \Delta T_{PWB} = \Delta T$, and the average shear strain is then dependent upon the CTE mismatch between the substrate and the printed wiring PWB. The shortcomings of equation (2.1) are: 1) assumes solder joints do not inhibit expansion of substrate and PWB; 2) no bending/warping of the substrate and PWB is included; 3) geometry of solder joint is neglected; 4) it provides an average value over the solder, rather than

specific values near the critical regions; 5) it does not account for the local CTE mismatch; 6) it does not take the geometry and angle of contact into consideration; 7) no creep or plasticity is taken into consideration;, 8) it does not take any of the intermediate solder balls into consideration which will affect.

Other analytical equations have been developed to overcome the shortcomings of equation (2.1). Suhir [3] improved upon Timeshenko's bithermostat beam theory [4] to develop one of the most popular analytical approaches for determining thermal stress in an electronic package. Wen and Basaran [5] introduce a multi-layered analytical model with orthotropic properties, interfacial compliance, and thermal loading. Wong et al. [6] present an analytical method for a CBGA that accounts for plasticity and the dual material structure of the solder joint.

2.1.2. Numerical Modeling:

The most basic numerical models are two dimensional, use linear elastic material properties, and have a low computation time [7]. However, they are also the most prone to being incorrect [8]. A 2D plane strain assumption provides a lower bound and 2D plane stress assumption provides an upper bound for 3D modeling results [9]. The best models in literature are 3D quarter models, include plasticity and creep material properties, and may use a submodeling [10, 11] or sub-structuring [12] approach for computational efficiency. Other well documented models are the 3D strip or Generalized Plane Deformation (GPD) model which is a compromise between 2D and 3D [9]. The stress free temperature is usually taken as the reflow or underfill cure temperature as it provides a more conservative estimate of the fatigue life [9].

Numerical modeling of large area array packages (>1000) solder joints, requires special consideration as it is computationally too intensive to model every solder joint. An effective approach has been to create a global 3D quarter model with the solder joints represented as equivalent beams and to use shells to model the substrate and PWB. The

deformations and temperature results from a specified boundary of the global modeled are then transferred to the boundaries of a detailed local model of a solder joints. Corbin [13] is one of the first researchers to fully show the advantages of the equivalent beam approach. However, using SHELL elements prevents the modeling of a die, aluminum lid, or heat sink because SHELL elements cannot represent the stacked structures. A layered SHELL can represent the stacked structures. However, it is then difficult to connect other components such as solder joints at the external faces of the layered shell elements. Other researchers have enhanced the approach by using SOLID elements to replace the SHELL elements. This allows for additional modeling of die, lids, heat sinks, etc… No known researcher has included the creep properties in the beams, and thus a significant contribution to deformation and damage is neglected in the global model [11].

2.1.3. Experimental Test:

Observing solder joint failure in most field environments is not practical in the design stage due to length of time it would take to achieve failure, typically on the order of years. Instead, Accelerated Thermal Cycling (ATC) tests are performed where the component is placed in a thermal oven and cycled at an accelerated rate and at greater temperature extremes. The danger of ATC tests is that a new or different failure mechanism than what is experienced in the field could be introduced due to the faster ramp rates and greater temperature extremes [14].

Test vehicles are designed so that the electrical resistance of the solder joints can be monitored to determine when failure occurs, usually when one joint fails. Definition of failure is often defined as an increase in resistance (in the range of 20 to 100% increase), or a 300 Ohm increase [15]. Cross-sectional analysis is used to confirm solder joint failure and not another failure mechanism.

2.1.4. Validation of Analytical and Numerical Models

In addition to validating the predicted life against experimental mean fatigue life, analytical/numerical models can be validated using other experiments as well. It is best to validate that the analytical/numerical models are capturing the correct mechanical behavior and that modeling material properties are correct. This can be best done through: (1) Laser Moiré Interferometry to validate material properties, in plane deformation patterns, and strain gradients [16-18], (2) Shadow Moiré Interferometry to validate out of plane warpage [19], or (3) Failure analysis of failed solder joints in ATC tests to validate predicted failure locations and mechanisms[20].

2.1.5. Acceleration Factor:

An Acceleration Factor AF is used to relate the mean number of cycles to failure N_{50} in the ATC tests to the N_{50} in the actual field environment. The most common equation is the Norris-Landzberg equation [21] shown in equation (2.2).

$$AF = \frac{N_{50a}}{N_{50b}} = \left(\frac{\Delta T_b}{\Delta T_a}\right)^{1.9} \left(\frac{f_a}{f_b}\right)^{1/3} e^{1414\left(\frac{1}{T_{peak,a}} - \frac{1}{T_{peak,b}}\right)} \tag{2.2}$$

where N is the mean number of cycles to failure, ΔT is the temperature range, f is the frequency in cycles per hour (cph), and T_{peak} is the maximum temperature in Kelvin. The subscripts a and b, relate to two different ATCs, and therefore, knowing N_{50a}, N_{50b} can be determined. The Norris-Landzberg equation has been shown to be valid for ceramic and plastic packages with Pb containing solder [10].

2.2. POWER CYCLING

Every electronic package has a chip that is powered and thus dissipates heat through joule heating. This heat is removed from the chip through two primary paths; (1) the front side of the chip consisting of the 1st level interconnects, the substrate, the 2nd level interconnects, and finally through the PWB, (2) The backside of the chip where some a heat sink or other means of cooling the chip is present. Because the chip acts as a heat

source, temperature gradients develop in the package and the expansion of the substrate and PWB is not as easy to predict as in the isothermal thermal-mechanical loading environment.

2.2.1. Analytical Modeling

Most of the analytical methods focus on determining the thermal performance and temperature gradients in the package. Approximations of the temperature changes in the substrate and PWB can be found by setting up a network of resistors representing the heat transfer paths. Equation (2.1) can then be used to find the shear strain. Gromman [22] performs a one-dimensional heat transfer analysis on a CBGA to find the temperature gradients. Bar-Cohen and Krueger [23] employ a 'star-network' that more accurately takes into account other heat transfer paths for calculating the junction temperature. Vinke and Lasance [24, 25] expand upon Bar-Cohen's method by adding coupling resistors and present the results for various packages, including a CBGA. Zemo and Kwon [26] compared the methods of Bar-Cohen, Lasance, and 3D numerical modeling to each other.

Once the temperatures (or an averaged temperature) of the substrate and PWB are found, Eq. (2.1) can be used as a first order estimate of the shear strain. A more comprehensive approach by Sundarajan et al. [27] includes plasticity and creep properties of solder and incorporates a crack growth approach to predict the fatigue life.

2.2.2. Numerical Modeling

Solving for solder joint fatigue in power cycling first involves a thermal analysis to solve for the temperature distribution and then a thermal-mechanical solution to solve for the displacements. Researchers [28] are using a compact thermal model as developed by Lasance [25] to simplify the thermal modeling of packages. Lasance's approach for compact thermal models has been implemented into the numerical modeling software FLOTHERM.

Modeling the convective boundary conditions can be a challenge as it is highly dependent upon how the airflows over the package [29]. In some situations such as multiple chips on a substrate [30], a fluid analysis must first be done to determine the convection coefficients. However, for most cases assuming a constant convection coefficient on the back side of the chip can simplify the model and still provide accurate results [31].

Material property characterization of the thermal conductivities is very important. The presence of copper vias and traces in the PWB introduces makes it difficult to model the PWB accurately [32]. The problem is simplified by assuming homogenous properties for the PWB through a rule of mixtures to determine isotropic properties, or better yet, to determine orthotropic properties [33]. A homogenous layer is also determined for the first level C4 interconnect layer. The thermal conductivity properties are crucial to correct prediction of temperature and displacement distributions [32, 34].

Most studies assume a uniform power distribution on the chip for simplicity. Yuan and Hong [35] showed that the assumption of a uniform power distribution on the chip is invalid for high power applications. The chip resistance can be over 2x higher for a nonuniform power distribution, resulting in higher temperatures and greater deformations leading to lower solder joint fatigue life. In addition the substrate and cap material play in important role in solder joint fatigue life.

2.2.3. Experimental Tests

Power Cycling tests are performed by cycling power to an active die and incorporating a cooling scheme on the back side of the chip. The power supplied ranges from 0.5W to 100W depending upon the type of package and application. Designing a test vehicle with an active die can be cost prohibitive, so Peltier devices are often used [36]. The disadvantage of a Peltier device is that it does not share the same mechanical properties as a silicon die and may lead to a different warpage of the package than if a silicon chip was used. An alternative to Peltier devices is to use resistors etched in the silicon die or

diodes as heat source. The cooling scheme typically consists of a heat sink with controlled air flow for convection cooling, or a cold plate is used for a more controlled test. Thermocouples placed strategically measure the chip temperature (junction temperature), heat sink temperature, and PWB temperature. Ideally, other thermocouples are used to determine solder joint temperatures and temperature gradients in the substrate and PWB. Alternatively, an infrared imaging camera can be used to get a more accurate view of the thermal profile.

2.2.4. Validation of Analytical and Numerical Models

Validating of power cycling models consists of first validating the temperature distribution determined from the thermal solution, and then validating the thermally induced displacements. The temperature solution can be validated by comparing the thermocouple readings or infrared images to the temperature results of the thermal solution [14, 37]. The junction temperature between the chip and substrate, T_j, is most commonly used as verification of the thermal solution[22]. Calculating and comparing the thermal resistance, R_{int}, between the chip and ambient temperature is also common way of validating the thermal models [33, 38]. Andrews [39] suggests that the thermal resistance, R_{int}, alone is not sufficient, as it depends on no less than 8 other constants, making it difficult to quantify R_{int} under different conditions.

A European consortium known as DELPHI has spent considerable time to get component manufacturers to supply validated thermal models of their parts [40]. In order to do this, DELPHI has established specific experimental procedures [41] using a double cold plate to verify numerical models with experimental tests. The method of cooling is specified because it plays a large factor in the thermal performance of the package, and the ability of the numerical model to capture the correct behavior.

Validating the displacements through Laser Moiré Interferometry is difficult in a PC environment where the chip must be kept whole, unless it is designed to still functional

when cross-sectioned [42]. If the numerical model has been validated for a thermal-mechanical loading and the thermal solution has been validated, then it may be safe to assume the displacements from the power cycling are correct.

2.2.5. Acceleration Factor

The Norris-Landzberg AF is only applicable when using it to predict fatigue life within the same environment, i.e. ATC to ATC or PC to PC. However, many researchers are incorrectly using the Norris-Landzberg AF to predict PC fatigue life from ATC fatigue life [43, 44]. Wakil and Ho [38] attempted to simulate power cycling tests with thermal cycling tests, however Engelmaier [45] and other researchers [37, 46] have concluded it is not possible to simulate the deformations that occur in power cycling with thermal cycling experiments. The problem lies in the fact that ATC conditions lead to an isothermal package and PC conditions lead to a non-isothermal package [36-38, 46, 47]. For ATC conditions: $\Delta T_{SUB} = \Delta T_{PWB} = \Delta T$, and for PC conditions: $\Delta T_{SUB} > \Delta T_{PWB}$ and Eq. (2.1) stays as is.

The question of whether γ_{ATC} or γ_{PC} is greater depends on the how close the substrate CTE, α_{sub}, matches the PWB CTE, α_{PWB}, which typically has a range of 18-24 ppm/C. For ceramic packages $\alpha_{sub} < \alpha_{PWB}$ so that $\gamma_{ATC} > \gamma_{PC}$. For ceramic packages, ATC tests lead to conservative estimates of PC fatigue life. Park et al. [48] performed numerical analysis and laser moiré experiments and have shown that PC can be more detrimental for PBGA while ATC is more detrimental for CBGA. Hong and Yuan [30] used FEM to study CBGA and found that ATC conditions can be 6-19x more conservative than PC conditions. Martin et, al. [49] performed experimental tests on a CCGA and found ATC conditions to be at least 4x more conservative than PC conditions. From a reliability point of view this is good, however it may lead to over designed, expensive packages [50]. There is a need for a new AF that can relate ATC fatigue life to PC fatigue life more accurately in order to avoid over designing packages.

When isothermal ATC conditions and non-isothermal power cycling conditions occur simultaneously then there is an additional complicating factor of two different frequencies and the Norris-Landzberg AF is not applicable according Galloway et.al, [51] who looked at several AF's for telecommunication applications.

2.3. VIBRATION ENVIRONMENT

Random vibration is the most common vibration environment experienced by most electronic packages [52]. Drop/shock impact is receiving much more interest with the rise of portable electronics. However, before these complicated environments can be fully understood some basic properties of the system need to be characterized. Much can be learned about the dynamics of a system through harmonic sinusoidal vibrations before more complex random vibration or drop/shock impact environments are explored. The vibration environment considered in this proposal is harmonic sinusoidal applied displacements.

2.3.1. Analytical Modeling

Analytical models can help to quickly identify the parameters of interest in vibration analysis early in the design process and are computationally less intensive than numerical models[53]. However, developing an analytical model that captures the correct fundamental frequencies, mode shapes, and stresses of individual solder joints is difficult. Modeling the correct boundary conditions is the most to getting accurate estimates of dynamic characteristics [53, 54]. Steinberg's book [55] is well known for its simple and rough estimates of system characteristics. Suhir [56, 57] has developed models to assess vibration-induced failures in electronic packages using a beam on elastic foundation. The solder joints are treated as a uniform layer so capturing stresses in the solder joints is not feasible. Singal and Gorman [58] have developed a general analytical solution for free vibration of rectangular plates resting on fixed supports and with attached masses. Barker et al. [53] model the interconnects as linear axial springs, however the curvature

of the PWB is assumed constant and thus only surface mounted components with peripheral joints are applicable.

2.3.2. Numerical Modeling

Compared to analytical models, numerical models are capable of representing the geometry, the material behavior, and the boundary conditions more accurately, and are capable of capturing the full spectrum of modes. However, as numerical models are computationally expensive [53], certain simplifying assumptions are needed to reduce computational time. Pitarresi et al. [59] have employed the 'smearing' technique to simplify numerical models. The majority of studies have focused on capturing mode shapes and natural frequencies of a circuit PWB, and not specifically on solder joint fatigue failure. Most studies reduce the electronic components to point or distributed masses. Only in recent years, have researchers begun including the details of the solid joints in order to capture fatigue behavior. Global-local or submodeling approaches such as the ones employed by Corbin [13], Hsu et al., [60], Yang et.al. [61], and Che et al. [62] are other techniques for representing detailed solder geometries without being computationally expensive.

2.3.3. Experimental Tests

Harmonic sinusoidal vibration tests are performed on electrodynamic shakers capable of sweeping from 1-2000Hz with a maximum acceleration of 10G's. Accelerometers are strategically placed to capture mode shapes and resonant frequencies of the system. There are a variety of boundary conditions used to fix the circuit PWB ranging from standoff screws, wedge clamps, stiffening fixtures, and clamping the edges of the PWB [55]. Care must be taken in designing the test vehicles as placement of the components on the PWB has a significant effect on mode shapes and natural frequencies of the system [61, 63]. In fact, much of the experimental work in literature has focused primarily on determining the mode shapes and fundamental frequencies of a circuit PWB with

multiple components. Pitarresi et al. [59, 64, 65] have done experimental work to characterize the natural frequencies, mode shapes, transmissibility, and damping at the PWB level. Only in recent years, have researchers such as Pang et. al. [7], Yang et al. [61], Li [66], and Wong et al. [67] have experiments and modeling the details of the solder joint to predict solder joint life due to vibrations.

2.3.4. Validating of Analytical and Numerical Modes

Comparison of predicted fundamental frequencies with experimental fundamental frequencies is the most common way to validate analytical/numerical models [61]. Increasingly difficult, but necessary, is validating mode shapes and accelerations [61, 68]. A less favorable way is to compare strain gauge measurements placed near the desired components [69].

2.4. COMBINED AND SEQUENTIAL THERMAL-MECHANICAL, POWER CYCLING, AND VIBRATION ENVIRONMENTS

Solder joint reliability under multiple environments can be tested under concurrent or sequential conditions. Literature is scarce on predicting solder joint fatigue failure under combined or sequential loading environments. Typical only two of the three environments are performed in combination or sequentially. Syed [12] looked at thermal cycling, power cycling ,and bending (not true vibration) for BGA package however it was not combined nor sequential loading. Nickerson and Desai [70] also looked at the individual effects of thermal cycling, power cycling, and bending for a PBGA. Basaran et al. [71] and Zhao et. al. [72] performed concurrent thermal and vibration test on a BGA and determined inelastic effects are important in vibrations.

Few standardized tests address the issue of assessing reliability under multiple environments, partly due to the complexity of the problem. Testing approaches that do involve multiple environments such as Highly Accelerated Life Testing (HALT), Highly Accelerated Stress Testing (HAST), and Multiple Environment Overstress Testing

(MEOST) are meant for quickly identify possible failure modes, and may not necessarily give an indication of reliability or a means to predict reliability.

Vibrations typically occur in the order of 5-2000 Hz while thermal cycling occurs at 5E-4 Hz. This time scale difference makes it difficult to model a combined load environment as it is too computationally intensive to simulate the over 10,000 vibration cycles that would occur over one thermal cycling. Instead, the vibration loading is performed at the maximum temperature of the thermal cycling where it is assumed the maximum damage will occur problem for combined vibration and thermal cycling [70].

In sequential loading of environments, the sequence in which the environmental loading is applied will also play a role in the solder joint fatigue life. This sequence effect should be understood in order to ensure the solder joint reliability is properly predicted. For example, IBM [52] and Ghaffarian [73] evaluated whether vibrations would have any significant degradation on subsequent thermal cycling for ceramic ball grid arrays (CBGA) and ceramic column grid arrays (CCGA). However, the effect of thermal cycling on subsequent vibration loading was not evaluated. Additionally, some standardized tests such as JEDEC JESD22-A113E and Military Standard MIL-STD-202F require preconditioning with ATC to simulate transportation conditions. This preconditioning could have significant effects on subsequent vibration loading and should be understood as some tests require it and others do not. Developing a predictive fatigue model that can account for the effect of sequence is important for components experiencing multiple environments.

CHAPTER 3

RESEARCH GAPS, RESEARCH OBJECTIVES, AND THESIS OUTLINE

3.1. RESEARCH GAPS IN EXISTING BODY OF LITERATURE

In light of literature review above, the notable gaps for Pb and Pb-free electronic packages to be addressed are:

1. No known 3D finite element modeling of large area array packages (>1000 solder joints) with creep included for each solder joint is present in existing literature. The models are either 2D or elastic-plastic solder or grossly simplifying submodels. In addition, the existing submodels ignore creep effects in the global model. This has two consequences (1) Warpage of the package is overestimated in the global model, as solder relaxation due to creep at higher temperatures is not included. (2) The contribution of creep damage to the damage parameter is underestimated and will lead to inaccurate solder fatigue life estimates.
2. No unified finite-element model is reported in the literature that models large area array packages under thermal, power cycling, and vibration environments. Separate FEMs are typically constructed for each loading environment due to variations in element types and capabilities for each environment. Although such an individual model may be appropriate for such an individual model may be appropriate for studying solder damage under one environment, it is not appropriate for studying solder damage under the application of all three environments. This is because calculation and comparison of damage parameters may be inconsistent among the three models because element mesh density, element type, material representation, and boundary conditions will vary among the three models. For example, in some existing literature vibration models, the packages are reduced to point masses and the solder joints are modeled as an elastic layer. However, to accurately predict the solder joint fatigue failure due to vibration, the package and solder joints must be modeled in detail. Therefore, modeling methodologies should be developed such that

a single geometry and material model can account for all loading environments and can enable calculation of damage from sequential or combined environments.

3. There is a need to better understand how fundamental vibration properties of large area array electronic packages affect the solder joint fatigue life. Due to their large mass and stiffness, large array area packages can significantly affect the vibration characteristics of the PWB and make location of the components a critical issue.

4. No known design based solder joint predictive equations for an area array package under thermal and power cycling,. In addition, the predictive equations that have been developed are not general enough to be used by other researchers and non-reliability experts, thus each researcher must develop their own equations.

5. No known Acceleration Factor exists for accurately predicting PC solder joint fatigue life from ATC solder joint fatigue life tests. Given the same temperature extremes and package geometry, PC tests and ATC tests will give different fatigue lives. The Norris-Landzberg AF does not take into account the difference between the ATC tests that do not have thermal gradients in the packaging assembly, and PC tests that have thermal gradients in the packaging assembly.

6. Solder Fatigue life under combined and sequential environments for electronic packages is poorly understood. Literature data is scarce on investigating solder joint fatigue life with experimental data or finite element models due to the complexity of the issue and expense of performing experimental tests. At best, a crude first order estimate using Miner's Cumulative Rule [74] is presently being used to predict solder fatigue life under sequential or combined environments. Miner's Rule has two primary faults; 1) it is insensitive to the sequence of load steps, and 2) it is typically non-conservative and overestimates fatigue life due to its linear nature.

3.2. RESEARCH OBJECTIVES

Given these gaps in existing literature, this thesis aims to develop a general unified modeling methodology to study the reliability of electronic packages subjected to thermal cycling, power cycling, and vibration loading conditions. Such a modeling methodology will comprise of an enriched material model to accommodate time-, temperature-, and

direction-dependent behavior of various materials in the assembly, and at the same time, will have a geometry model that can accommodate thermal- and power-cycling induced low-cycle fatigue damage mechanism as well as vibration-induced high-cycle fatigue damage mechanism. This thesis aims to apply such a model to study the reliability characteristics of CBGA/CCGA packages with lead-based solder interconnections. In particular, this thesis will aim to study the reliability of such packages under thermal, power, and vibration conditions individually, and validate the model against these conditions using appropriate experimental data either from in-house experiments or existing literature data. Once validated, this thesis also aims to perform a design of simulations study to understand the effect of various material, geometry, and thermal parameters on solder joint reliability of CBGA and CCGA packages, and use such a study to develop universal polynomial predictive equations for solder joint reliability. The developed predictive equations will be grounded in the mechanics of material behavior and at the same will be easy enough to be used by a wide range of engineers and experimentalists without extensive background in mechanics and/or finite-element modeling. The thesis also aims to employ the unified modeling methodology to develop new understanding of the acceleration factor relationship between power cycling and thermal cycling. Finally, this thesis plans to use the unified modeling methodology to study solder joint reliability under the sequential application of thermal cycling and vibration loading conditions, and to validate the modeling results with first-of-its-kind experimental data.

Figure 3-1 presents a schematic of how the components of the unified modeling methodology fit together.

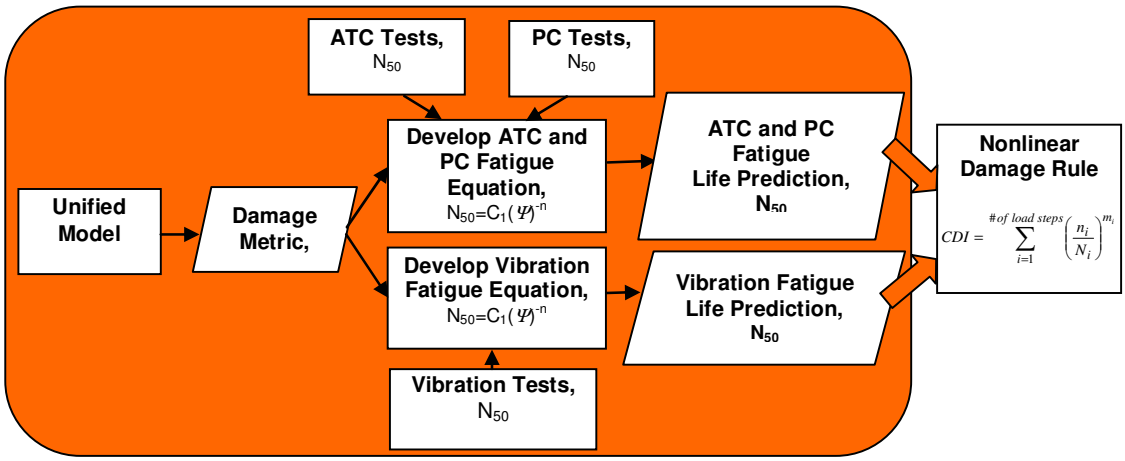


Figure 3-1. Unified Modeling Methodology

From Figure 3-1 it is seen that a damage metric is derived from the unified model. The choice of damage metric will depend on whether the loading is a low-cycle ATC/PC or high-cycle vibration environment. The fatigue equations are derived by relating experimental fatigue life data to the damage metric. Once the fatigue life equations are derived they can be used in combination with the developed nonlinear cumulative damage rule to predict the fatigue life under sequential environments.

3.3. THESIS OUTLINE

The thesis is outlined according to the following chapters. Chapter 4 will provide background material into CCGA/CBGA electronic packages, solder material behavior and modeling, laser moire interferometry, power cycling, and vibration analysis. Chapter 5 will develop the unified FEM for thermal cycling, power cycling, and vibration environments for CCGA and CBGA packages. Chapter 6 will validate the unified FEM for ATC and PC environments by comparing the predicted deformation and temperature gradients against laser moire interferometry and power cycling experiments. Chapter 7 develops the predictive solder joint fatigue equations for CBGA and CCGA electronic packages under ATC and PC by using in-house and literature experimental fatigue life data. Chapter 8 validates the unified FEM for vibration environments and develops a fatigue life prediction equation for CCGAs under vibration loading. Chapter 9 illustrates

the methodology of developing a universal polynomial predictive equation for solder joint reliability of a CBGA under ATC environment. Chapter 10 uses the methodology of chapter 9 to develop a universal polynomial predictive equation for PC. An AF to relate PC to ATC is then developed by using the ratio of the PC and ATC universal polynomial predictive equations. Chapter 11 develops a nonlinear cumulative damage rule that accounts for the sequence effect of multiple environments. Chapter 12 provides research contribution and suggestions for future work.

CHAPTER 4

BACKGROUND

In order to understand how to predict solder joint reliability for ceramic area array packages under thermal cycling, power cycling, and vibration loading, then some background material is necessary. The background material covered in this chapter includes: the fundamentals of ceramic area array packages; solder material behavior and modeling; laser moire interferometry; and fundamentals of vibration theory relevant to electronic packages.

4.1. CCGA AND CBGA ELECTRONIC PACKAGES

CBGA and CCGA packages have gained popularity for high I/O applications due to their proven thermo-mechanical reliability and fairly standard assembly techniques. Figure 4-1 shows a cross-section of a CCGA. The CBGA has a similar construction as the CCGA, except a 90Pb10Sn solder ball is used rather than a 90Pb10Sn solder column. For a 1.27mm pitch, CBGA packages use a 90Pb10Sn high lead solder ball (.89 mm dia.) with 63Sn37Pb eutectic solder fillets. For a 1.27mm pitch, IBM's CLASP (Column Last Attach Process) CCGA packages use a high melting point 90Pb10Sn solder column (2.21 mm high) with a palladium (Pd) doped 63Sn37Pb solder fillet on the substrate side and 63Sn37Pb solder fillet on the board side. The CLASP structure allows for the columns to be attached last as the substrate side Pd doped 63Sn37Pb fillet has a slightly higher reflow temperature than the board side 63Sn37Pb fillet (183^0C). This allows the columns to be attached to the board without reflowing the connection on the substrate side. The 90Pb10Sn columns have a reflow temperature of 275^0C, which allows a constant stand-off height to be maintained during attachment of the substrate to the board. IBM offers the solder columns in 2.21mm and 1.27mm heights.

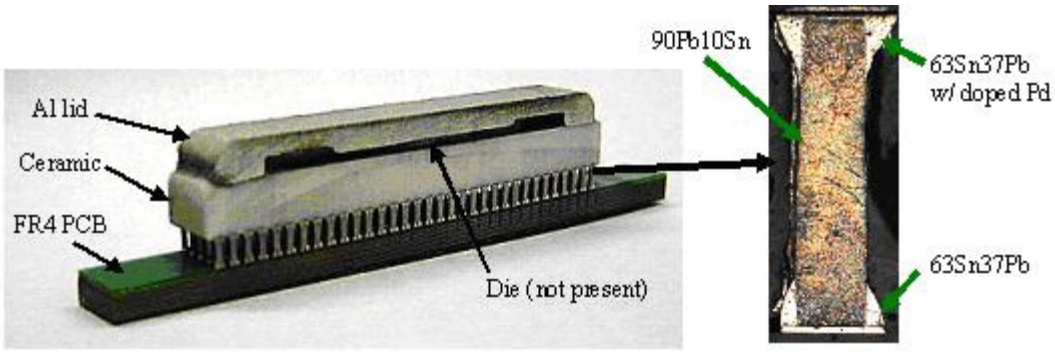


Figure 4-1. Cross-section of a Ceramic Column Grid Array (CCGA).

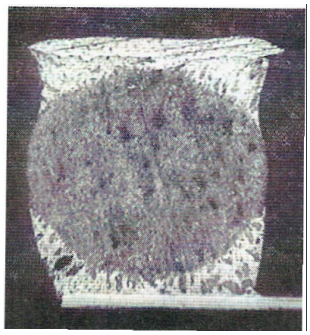


Figure 4-2. Cross-section of a CBGA with 0.89mm diameter 90Pb10Sn ball [75].

Table 1 compares the advantages and the drawbacks of the two packages. In general, the CBGA is preferred over the CCGA due to easier processing and better electrical properties [2].

Table 4-1. Comparison of CBGA and CCGA

	CBGA	CCGA
Advantages	Standard Processing Tools Less vertical space used Better dynamic-mechanical reliability Lower inductance, capacitance, (verify CBGA IBM manual) Good self-aligning characteristics	Better thermo-mechanical reliability Higher I/O counts >1657
Disadvantages	Lower thermo-mechanical reliability Limited to I/O <1657	Non-standard assembly process Large vertical space required Limited dynamic reliability

From a thermo-mechanical reliability point of view, CCGA packages are preferred over CBGA packages due to the increased stand-off height of the solder column allowing better accommodation of the CTE mismatch between the substrate and the board [3].

Current CCGA packages on a 52.5x52.5 mm substrate with 1.00 mm pitch allow for 2577 I/Os. From a process and assembly point of view, CBGA packages are preferred due to their use of standard processing tools. Unfortunately, CBGA packages are currently limited to 1657 I/Os on a 42.5x42.5 mm HITCE glass ceramic substrate with 1.00mm pitch.

Table 2 lists the number of I/Os available for specific substrate sizes at pitches of 1.27mm and 1.00mm. The 1.27mm pitch removes one corner solder joint for identification purposes. The 1.00mm pitch removes six I/Os in each corner for handling purposes. Decreasing the pitch from 1.27mm to 1.00mm allows up to a 1.6x increase in the number of I/Os for a specific body size, or maintaining the same number of I/Os but going to a smaller substrate size.

Table 4-2. I/Os available for substrate size and pitch

Substrate Size (mm)	Pitch (mm)			
	1.27		1.00	
	Array	I/Os	Array	I/Os
52.5x52.5	40x40	1588	51x51	2577
42.5x42.5	33x33	1088	41x41	1657
32.5x42.5	25x33	824	31x41	1247
32.5x32.5	25x25	624	31x31	937
25x32.5	19x25	474	25x31	800
25x25	19x19	360	25x25	600

For packages with 600-1000's I/Os, one can choose between a CBGA or CCGA package. The decision will be based on the application and the existing design requirements. For example, a CCGA may be desirable for its higher thermo-mechanical reliability, but takes up too much vertical space, so a CBGA package must be used. However, the CBGA package may not meet thermo-mechanical fatigue life requirements for applications in harsh environments.

The thermo-mechanical fatigue life can be improved by using a glass ceramic (HITCE) substrate with a Young's modulus of 74 MPa and a CTE of 12.3 ppm/^{0}C to better match

the organic FR4 CTE of 18-22 ppm/^{0}C. A HITCE ceramic substrate has been published for CBGA packages [4,5,6,7], but not for CCGA packages.

4.2. CCGA TEST VEHICLE DESCRIPTION

The CCGA test vehicles used in the ATC and vibration tests are 42.5mm x 42.5mm x 4mm CCGA electronic packages with 1089 solder joints. Six CCGA's were assembled by Compaq onto 152.4x228.6x2.8mm thick FR4 printed wiring boards containing 8 layers of 0.5oz Cu. A 1.3mm thick aluminum lid was bonded to the ceramic substrate with Sylgaard adhesive. There was no die in the package. Georgia Tech received 6 such assembled boards. In order to maximize the number of available components for experimental purposes and make each board identical, the boards were cut into individual 137mm long x 56mm wide strips with a CCGA centered in each strip as shown in Figure 4-3.

Figure 4-3. CCGA test vehicle on 137mm x 56mm x 2.8mm FR4 board

The CCGA solder joints are electrically daisy-chained with a total of ten daisy chains; nine rings (R_0-R_8) in which each of the daisy chain contains solder joints with similar distances from the neutral point (DNP), and one daisy chain (R_{XX}) that contains all solder joints that are not in daisy chains R_0-R_8. Due to limitations in the hardware available to monitor the daisy chain electrical resistance at a sampling rate greater than 10 KHz, only 3 of the 9 daisy chain rings were monitored. Figure 4-4 shows a layout of the R_0, R_1, and R_{XX} daisy chains that were monitored in this study. The array of solder joints is a 33x33 grid, and a notation of (row, column) will be used to identify individual solder joints. The (1,1) solder joint is located in the lower right hand corner. The solder joints marked

J_0 (1,1), J_1 (3,1), and J_{XX} (13,1), in Figure 4-4 will be used in subsequent sections to characterize daisy chain rings R_0, R_1, and R_{XX}, respectively in the finite element model (FEM).

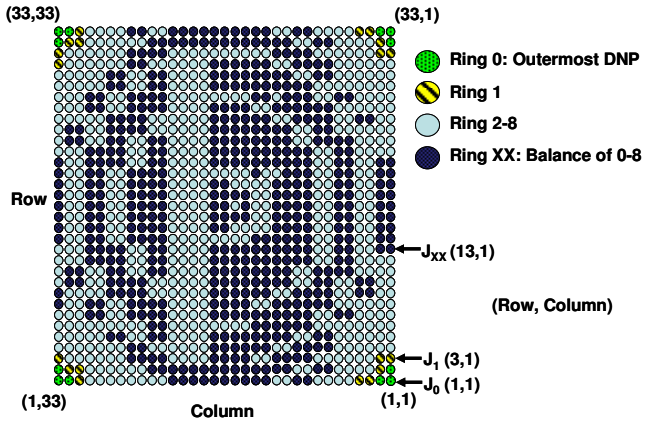


Figure 4-4. Electrically monitored daisy chain rings of CCGA

4.3. SOLDER MATERIAL BEHAVIOR AND FATIGUE

Solder has proven to be valuable as a mechanical and electrical interconnect material in the electronics industry primarily due to its low melting point, wetting behavior, electrical properties, and availability. Solder has also proven to be a very difficult material to understand as it exhibits such phenomena as age-and cycle softening, grain-growth hardening, strain-rate hardening, and "superplasticity" [76]. Despite over many decades of characterizing and modeling solder, there is still great difficulty in capturing and modeling its behavior. A very elementary view of solder will be reviewed in this section, primarily to enable one to understand how to choose the correct constitutive models that are available in most commercial finite element software such as ANSYS or ABAQUS.

4.3.1. Solder Behavior

Solder stress/strain behavior is traditionally broken down into three parts: an elastic strain portion ε_e; a time-independent plasticity strain ε_p; and a time-dependent creep strain ε_c. A simple rheological model for solder, shown in Figure 4-5, consists in a series connection

of a spring, a slider in parallel with a spring, and a damper, to represent the elastic, plastic, and creep portions respectively.

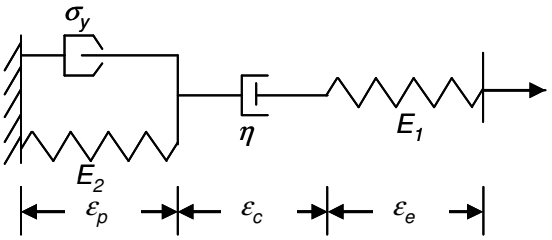


Figure 4-5. Rheological model representing solder behavior.

The rheoleogical model of Figure 4-5 will respond to a stress loading as shown in Figure 4-6.

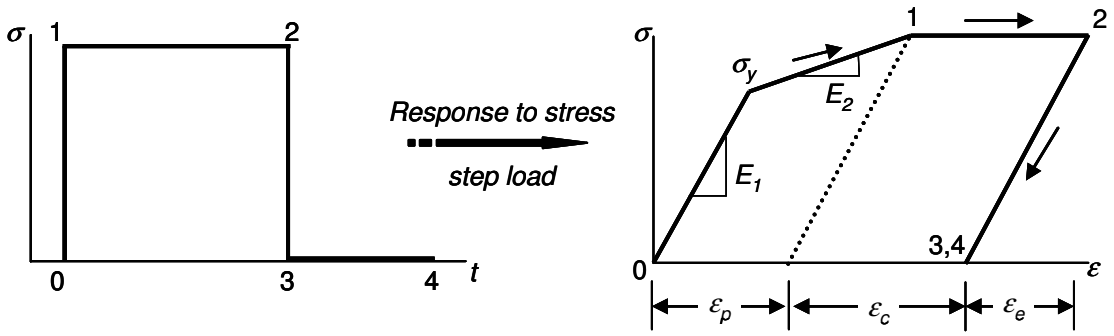


Figure 4-6. Stress-strain response for simple rheological model of solder to a stress step load.

The total strain is the sum of the three portions.

$$\varepsilon_{tot} = \varepsilon_e + \varepsilon_p + \varepsilon_c \tag{4.1}$$

The details and modifications to each strain portion will now be discussed. To simplify the discussion, the ideas will be presented in one-dimensional terms.

4.3.1.1. Elastic Strain

The spring in Figure 4-5 represents the recoverable elastic strain ε_e. The elastic strain follows Hooke's Law

$$\varepsilon_e = \frac{\sigma}{E} \tag{4.2}$$

where σ is the applied stress in MPa, and E is Young's Modulus in MPa. For solders, Young's Modulus is a temperature-dependent property.

4.3.1.2. Plastic Strain

Plastic strain is time-independent nonrecoverable deformation, typically due to dislocation pileups from lattice defects. As a material is loaded up to a specified strain level, the stress rises linearly until it reaches the yield stress σ_y at which plastic deformation begins to occur. Figure 4-7 shows three typical ways of modeling plasticity; perfectly plastic, elastic linear hardening, and nonlinear hardening.

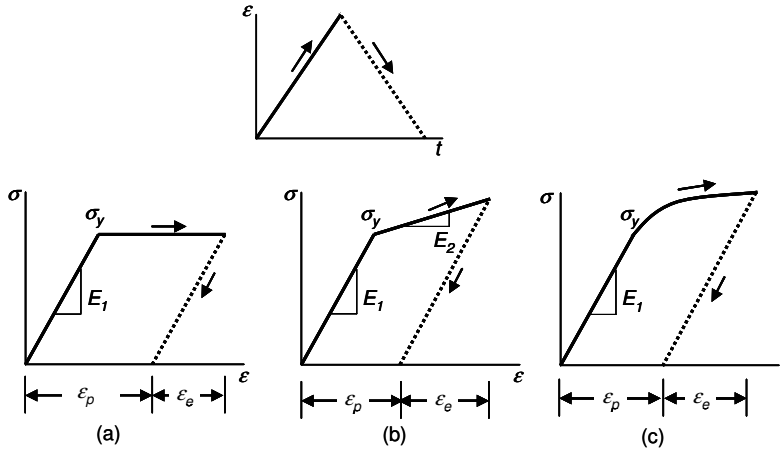


Figure 4-7. (a) Perfectly Plastic. (b) Elastic linear hardening. (c) Nonlinear Hardening.

Solder plasticity is best modeled with a nonlinear hardening model during loading as shown in Figure 4-7(c). A common constitutive model for nonlinear hardening plasticity is the Ramgood-Osgood equation

$$\sigma = H\left(\varepsilon_p\right)^n \tag{4.3}$$

where H is a material constant set to be the stress value σ_y where ε_p=1, and n is a material constant called the strain hardening exponent.

The plastic behavior of solder is temperature dependent, specifically the yield stress σ_y. Figure 4-8 shows the behavior of 90Pb10Sn and 60Sn40Pb solder as a function of temperature.

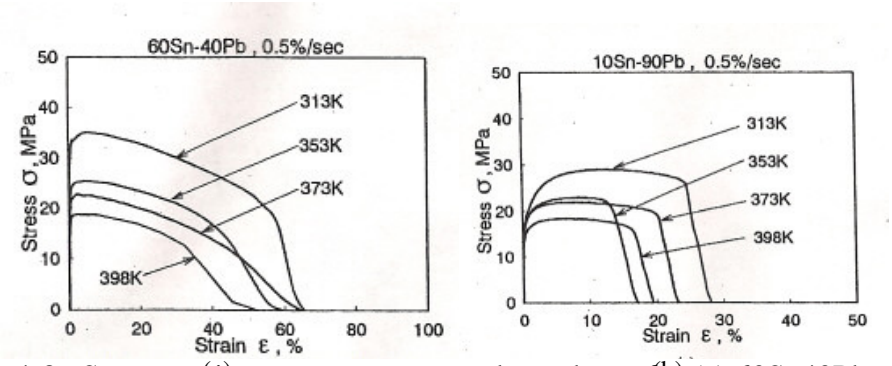


Figure 4-8. Stress-strain curve temperature dependence for (a) 60Sn40Pb and (b) 90Pb10Sn solders .[77]

The point at which yielding occurs upon reverse loading is also of interest. There are two main models that specify the point at which reverse yielding occurs; *multi-linear isotropic hardening* (MISO) and *multi-linear kinematic hardening* (MKIN). The difference between the two models is illustrated in Figure 4-9.

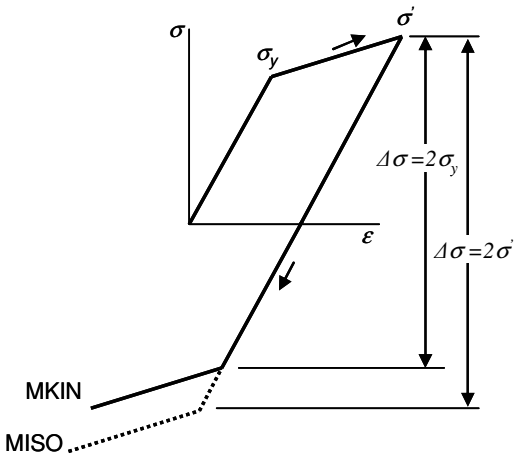


Figure 4-9. Reverse yielding showing multilinear kinematic hardening (MKIN) and multilinear isotropic hardening (MISO)

When a material is loaded beyond the yield stress σ_y up to a point σ' and then a reverse load is applied, the material will yield at $\Delta\sigma = 2\sigma_y$ according to MKIN, and at $\Delta\sigma = 2\sigma'$

for MISO. The MKIN model represents the Bauschinger effect that is observed in real materials such as solder [78, 79]. MISO does not characterize real materials very well. However, it is occasionally the only choice of modeling plasticity for some choices of elements in finite element software. This issue will be dealt with in more detail later.

4.3.1.3. Creep Strain

A metal will begin to exhibit creep behavior when its homologous temperature (percent of melting temperature on the absolute scale of Kelvin) is near or above 0.5. Eutectic 63Sn37Pb solder has a melting temperature of 183°C (456K) which makes its homologous temperature to be about 0.65 at room temperature. Creep strain accumulation is most easily demonstrated by holding a material under a constant stress over a long period of time and observing the deformation increase over time. There are typically three observable stages of creep as illustrated in Figure 4-10; the *primary* stage is often short and decelerating in nature, the *secondary* or *steady-state* stage is characterized by a constant strain rate, and finally the *tertiary* stage is unstable acceleration until rupture occurs [78].

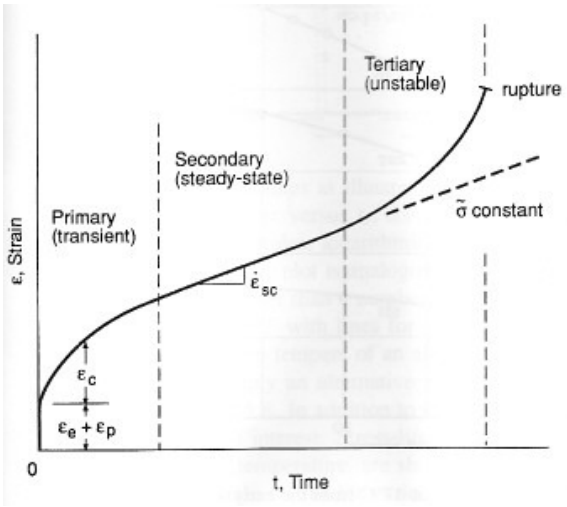


Figure 4-10. Primary, secondary, and tertiary stages of creep strain under a constant load. [78]

Most creep models deal with only the *steady-state* creep as that is where the majority of creep strain occurs. A damper as shown in Figure 4-5 is often used in a rheological model to model steady state creep.

The physical mechanism of steady-state creep in solder has been well-studied and in general has been observed to be a function of applied stress and temperature in which *dislocation glide* and *climb* cause vacancy and cavity diffusion. At low stresses and high temperatures *dislocation glide* dominates while at low temperatures *dislocation climb* dominates [12, 80] [81-83]. Figure 4-11 is a graphical representation of *dislocation glide* and *dislocation climb*. *Dislocation glide* is movement of an edge dislocation along a crystal lattice plane. *Dislocation climb* occurs when a particle or immobile obstacle is met and the dislocation must climb to another crystal lattice plane[78].

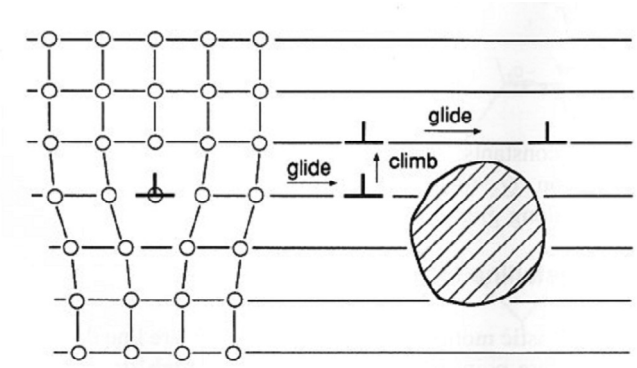


Figure 4-11. Climb of an edge dislocation permitting glide to continue. [78]

Three common constitutive models for steady state creep include:

1) an Arrhenius-type equation which is best for creep in the low stress range:

$$\dot{\varepsilon}_c = A_0 \sigma^n \exp\left(\frac{-Q}{R_G T}\right) \tag{4.4}$$

where A_0 and n are creep constants, Q is the activation energy for dislocation motion, R_G is the universal gas constant, $\dot{\varepsilon}_c$ is the creep strain, σ is the applied stress, and T is the absolute temperature.

2) a Garafalo hyperbolic sinh equation which does a good job of covering creep in the low to medium stress range:

$$\dot{\varepsilon}_c = A_0 [\sinh(\alpha\sigma)]^n \exp\left(\frac{-Q}{R_G T}\right) \tag{4.5}$$

where A_0 and n are creep constants, Q is the activation energy for dislocation motion, R_G is the universal gas constant, $\dot{\varepsilon}_c$ is the creep strain, σ is the applied stress, and T is the absolute temperature

3) a double power law equation which is indented to capture the dislocation glide and dislocation glide mechanisms [12, 84] in the medium and high stress regions.

$$\dot{\varepsilon}_c = A_1\left(\frac{\sigma}{E}\right)^{n_1} \exp\left(\frac{-Q}{R_G T}\right) + A_2\left(\frac{\sigma}{E}\right)^{n_2} \exp\left(\frac{-Q}{R_G T}\right) \tag{4.6}$$

where A_1, A_2, n_1, and n_2 are creep constants, Q is the activation energy for dislocation motion, R_G is the universal gas constant, $\dot{\varepsilon}_c$ is the creep strain, σ is the applied stress, and T is the absolute temperature

The strain rate affects the creep behavior of solder for strain rates below 2%/s [77]. For thermal cycling and power cycling the strain rate of loading is on the order of 10^{-4}%/s and creep is important. However, for vibration loading where the strain rate of loading is on the order of at 10%/s then creep effects are minimal and will not be included in constitutive models.

4.3.1.4. Cyclic Behavior under thermo-mechanical loads

Capturing the cyclic behavior of solder under thermo-mechanical loads is even more difficult than capturing the monotonic loading behavior described thus far. Figure 4-12 shows a typical accelerated thermal cycle with a choice of stress-free temperature as either the solder reflow temperature (183°C) or room temperature (20°C). The choice of stress-free temperature will be dealt with in section 5.2.6.

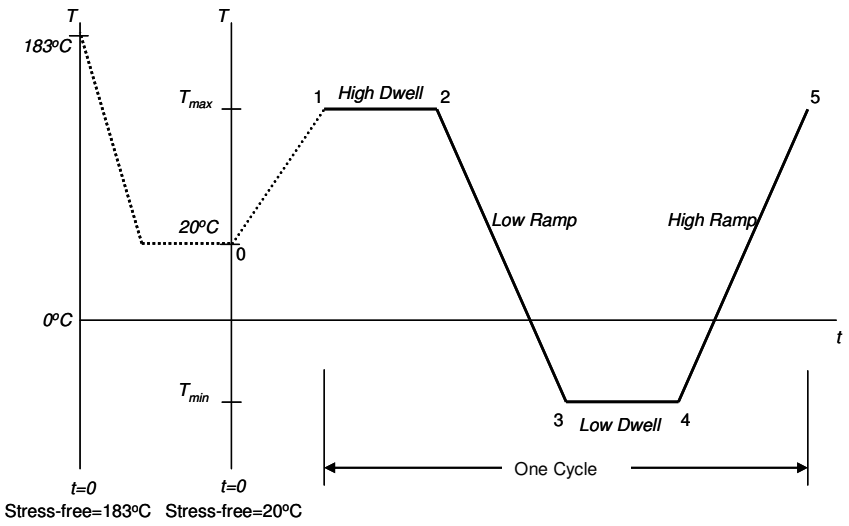


Figure 4-12. Typical accelerated thermal cycle (ATC) .

The cyclic response of a solder joint will depend on numerous factors, some of which are the composition of solder, structure of the joint, stress-free condition, temperature range, mean temperature, rate of loading, and time at dwells. Two commonly observed cyclic responses for solder are *shakedown* and *ratcheting* as illustrated in Figure 4-13. *Shakedown* is when the stress-strain hysterisis loop stabilizes by no longer changing shape and stops moving along the strain axis. *Ratcheting* occurs when the hysterisis loop may stabilize in shape but continues to travel along the strain axis. Ratcheting is typically due to creep and non-zero mean stresses [78, 85, 86].

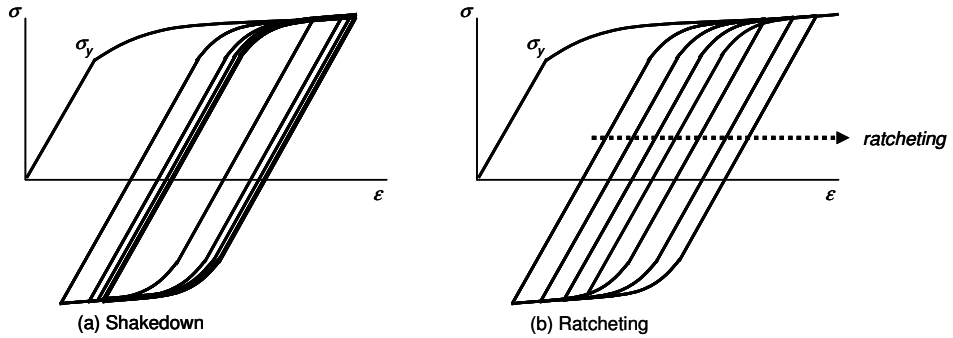


Figure 4-13. (a) Shakedown stabilization of stress-strain hysterisis, (b) ratcheting of stress-strain hysterisis loop due to mean stress effects.

As an example of a hysterisis loop, Figure 4-14 shows the shear stress-strain hysterisis loop predicted for the solder joint with the furthest distance from the neutral point (DNP) in a ceramic ball grid array (CBGA) package. The simulated ATC includes a cool down from the stress-free condition of 183°C followed by a 4 day dwell at 20°C. The ATC is 0/100°C at 2cph.

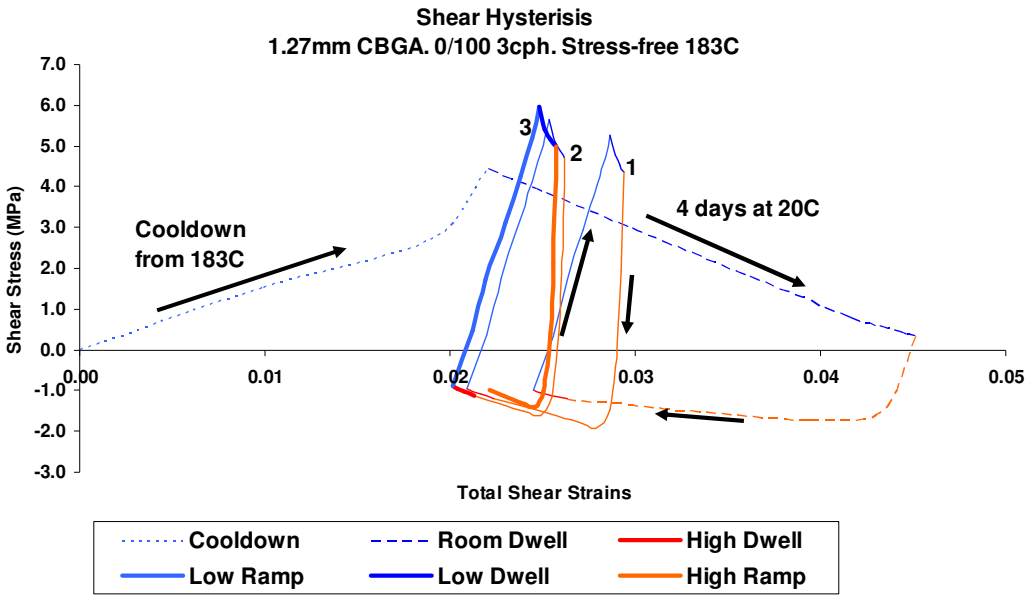


Figure 4-14. Stress-Strain hysterisis loop for CBGA under 0/10oC 2cph ATC.

Shakedown can be observed in Figure 4-14 where the stress-strain hysterisis loop stabilizes after three thermal cycles. Considerable creep strain and stress relaxation is observed during the 4 day dwell at 20°C. Once thermal cycling begins the highest shear stresses occur during the low ramp and low dwells. The largest strain accumulation occurs during the high ramps and high dwells where creep occurs due to the higher temperatures.

4.3.2. Damage Parameters

When predicting solder joint fatigue failure, a metric of the damage occurring, called a damage parameter, must be chosen. Figure 4-15 shows some common damage

parameters based on the stabilized stress-strain hysterisis loop: $\Delta\varepsilon_e$ is the *elastic strain range per cycle*; $\Delta\varepsilon_{in}$ is the *inelastic strain range per cycle* defined as the sum of the creep and plastic strain ranges per cycle; $\Delta\varepsilon_{tot}$ is the *total strain range per cycle* and is the sum of the elastic strain ranger per cycle $\Delta\varepsilon_e$ and the inelastic strain range per cycle $\Delta\varepsilon_{in}$; σ_a is the stress amplitude per cycle; ΔW_{in} is the *inelastic strain energy density per cycle* and is defined by the area of the stress-strain hysterisis loop where plastic and creep damage occur; ΔW_e is the *elastic strain energy density per cycle* and is defined by the area outside of the inelastic strain energy density per cycle. The sum of the inelastic strain energy density ΔW_{in} and the elastic strain energy density ΔW_e is the *total strain energy density per cycle* ΔW_{tot}. The strain energy density may also be called work in some texts.

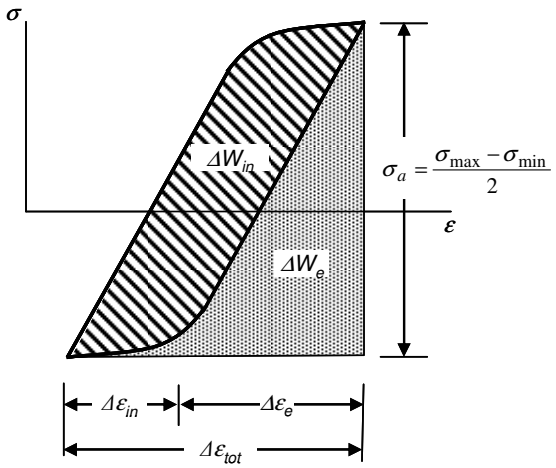


Figure 4-15. Stabilized stress-strain hysterisis loop showing common damage parameters.

4.3.3. Solder Joint Fatigue Failure Prediction

Traditional approaches for predicting solder joint fatigue use a fatigue equation with a physics-based damage parameter such as inelastic strain or total work. A Coffin-Manson type equation [87] is the most popular equation in literature for predicting solder joint fatigue

$$N_f = C_1(\Psi)^{C_2} \tag{4.7}$$

where: N_f is the fatigue life, in cycles, C_1 and C_2 are constants found through least squares regression, and Ψ is a damage parameter.

In order to predict the fatigue life, the constants C_1 and C_2 must be determined through least squares regression relating the fatigue life N_f and the damage parameter Ψ. The fatigue life N_f is obtained by performing experiments and is given as some percentage of failed samples, typically the mean life of 50% or characteristic life of 63%. At least two experiments need to be performed in order to determine the two constants. Ideally, more than two experiments would be run in which the design parameters and the loading environment are changed so as to ensure the fatigue life is accurately predicted as a function of design parameters and loading environment.

The damage parameter Ψ is a scalar quantity representing the damage that causes the fatigue failure. Common damage parameters relevant for solder joint fatigue are: Inelastic strain range per cycle [88], total strain range per cycle [82], accumulated creep strain per cycle [80], accumulated inelastic work per cycle, VonMises Stress range per cycle, inelastic work per cycle [89], and total work per cycle [90]. The choice of damage parameter will depend upon the loading environment and preference of the researcher. Inelastic strain range per cycle is the most common damage parameter for low cycle fatigue ($<10^4$ cycles) common in thermal-mechanical and power cycling environments. Total strain range per cycle and VonMises Stress range per cycle are most common for high cycle fatigue ($>10^5$ cycles) where inelastic strains do not play a major role. Lee et al. [91] provides a good review of the choice of damage parameters and fatigue models.

It is noted that there are many other damage models available. Dasgupta et.al. [92] use a micro-mechanics approach to account for microstructural changes and crack initiation under vibration and thermal cycling. Sayama et al. [93] use a microstructural evolution approach using grain growth as a damage parameter. Darveaux's approach of using

crack growth related to a volume-weighted average plastic work density [89] has gained considerable favor in the electronics packaging community. Darveux uses the sum of a crack initiation period in Eq. (4.8) and a crack growth period in Eq. (4.9) to predict the lifetime as shown in Eq. (4.10)

$$N_o = K_1(\Delta W_{ave})^{K_2} \tag{4.8}$$

$$\frac{da}{dN} = K_3(\Delta W_{ave})^{K_4} \tag{4.9}$$

$$N_f = K_1(\Delta W_{ave})^{K_2} + \frac{a}{K_3(\Delta W_{ave})^{K_4}} \tag{4.10}$$

where ΔW_{ave} is the accumulated plastic work density per cycle, N_o is the cycles to crack initiation, a is the final crack size, da/dN is the crack growth rate, and K_1, K_2, K_3,, and K_4 are material constants. Anand's model is used so the definition of 'plastic' in this case refers to inelastic.

Models based on continuum damage mechanics, disturbed state concept, or a thermodynamics framework such as McDowell [79], Stolkarts et al. [94], and Basaran and Chandaroy [47], are also popular however they are very difficult to implement. Sharma and Dasgupta [95] attempt to tie together the macroscale phenomenological models with microstructural and mechanistic modeling that takes into account grain boundary sliding, void nucleation, et.

4.4. CUMULATIVE DAMAGE PREDICTION: MINER'S RULE

Miner's cumulative linear damage rule [74] as shown in Eq. (4.11) is commonly used to predict fatigue life damage under multiple loadings/environments due to its simplicity:

$$CDI = \sum_{i=1}^{\#of\ load\ steps} \frac{n_i}{N_i} \tag{4.11}$$

where CDI is the cumulative damage index, n_i is actual number of applied cycles for the i^{th} load step, and N_i is the number of cycles to failure for the i^{th} load step. CDI ranges from 0 to 1.0 with 0 being the undamaged state and 1.0 being the fully damaged state.

Failure is typically defined when the CDI exceeds a critical value of 0.7 [55]. According to Eq. (4.11) in a two step loading when a damage ratio of n_1/N_1 is consumed, then the remaining second step has a damage ratio $n_2./N_2 = CDI - n_1/N_1$ before failure occurs.

Miner's cumulative linear damage rule has been used in solder joint reliability; Pang, et. al., [7] for fatigue failure of PBGA's under vibration loading at different accelerations, Perkins and Sitaraman [future ASME publication] for fatigue failure of CCGA's under vibration loading, Barker, et. al., [96] and Steinberg [55] for predicting fatigue life of electronic components under thermal and vibration loading, and Chih-Kuang and Hsuan-Yu [97] studied the sequence effect of high-low vs low-high stresses on the creep fatigue life of SAC solder.

However, the usefulness of Miner's rule due to its linear nature has been called into question for several reasons [98].

1. Insensitivity to sequence of load steps. The order of loading does not come into play in Miner's Rule. The effect of sequence can be important. For example, Lin and Teng [97] showed that for creep tests a high-low load sequence was more detrimental than a low-high load sequence. The sequence effect has been shown extensively for metals in general [99] [100].
2. Typically is non-conservative and overestimates fatigue life due to its linear nature. Many researchers simply lower the *CDI*, however this is somewhat arbitrary and inconsistent for different loadings.

Several damage models have been proposed as alternatives to Miner's rule. Basaran and Chandaroy [101] propose a unified damage mechanics based constitutive model for assessing solder joint fatigue under concurrent thermal and vibration loading. Crack initiation and crack propagation have been also been used as damage parameters by Manson [102] and Singh [98] to account for sequence effects and other abnormalities. However, such approaches do not always result in greater accuracy across a broad

spectrum of environments and loadings, and they require extensive material testing and a great number of experiments. Such extensive material testing and data gathering is often impractical for quick analysis of solder joint fatigue for microelectronic packages. A simpler approach is utilized according to Marco-Starkey [103] where an exponent is incorporated into the fatigue life ratio and set the *CDI* equal to one:

$$CDI = 1.0 = \sum_{i=1}^{\#\,of\ load\ steps} \left(\frac{n_i}{N_i}\right)^{m_i} \tag{4.12}$$

where m_i is a fitting parameter exponent that varies for each environment i and on the sequence of loads.

4.5. LASER MOIRE INTERFEROMETRY

4.5.1. Theory

Laser Moire Interferometry is an optical technique that uses the interaction of a crossed-line diffraction grating on the sample and four coherent beams to produce moiré fringes N_x and N_y which represent displacements in the horizontal U and vertical V directions respectively [104, 105]. The capability of laser moire to capture whole-field deformation and deformation of a single joint is vital for understanding how solder joints fail, and for verifying the behavior predicted in subsequent finite element models.

Figure 4-16 shows a schematic of the four beam laser moire interferometry setup.

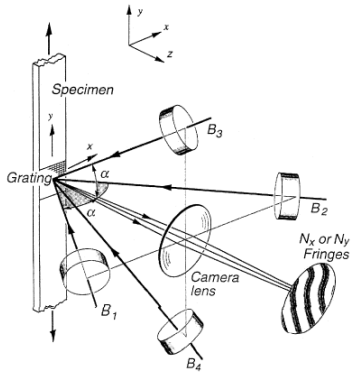


Figure 4-16. Schematic of four beam moire interferometry to produce deformation fringes Nx and Ny. [105]

With a cross-line reference grating of f_s=1200 lines/mm it is possible to determine the horizontal (U) and vertical (V) displacement fields down to a resolution of $1/2f_s$ = 0.417 μm. The number of interference fringes relates directly to the *U* and *V* displacements according to Eqs. (4.13) and (4.14).

$$U = \frac{N_x}{2f_s} \tag{4.13}$$

$$V = \frac{N_y}{2f_s} \tag{4.14}$$

where N_x is the number of fringes in the horizontal direction, N_y is the number of fringes in the vertical direction, and f_s is the frequency of the cross-line grating specified as 1200 lines/mm in this study

The corresponding normal strains, ε_x and ε_y, along with the shear strains γ_{xy} can be extracted by counting the fringes over the appropriate gage lengths Δx and Δy.

$$\varepsilon_x = \frac{\delta U}{\delta x} = \frac{N_x}{2f_s \Delta x} \qquad \varepsilon_y = \frac{\delta V}{\delta y} = \frac{N_y}{2f_s \Delta y}$$
$$\gamma_{xy} = \left[\frac{U}{\Delta y} + \frac{V}{\Delta x}\right] = \frac{1}{2f_s}\left[\frac{N_x}{\Delta y} + \frac{N_y}{\Delta x}\right] \tag{4.15}$$

4.5.2. Prior work on laser moire interferometry of CBGAs and CCGAs

Previous studies involving Bongtae Han et. al. [106] have used laser moire interferometry to study lead containing CCGA [107] and CBGA[108]. The work by Han et.al. provided important insight into the deformation behavior of CCGAs and CBGAs under thermal-mechanical loads. For example, Cho and Han [108] used real-time moire interferometry to characterize the deformation behavior of a CBGA under the thermal loading. By observing the whole-field deformation patterns at various temperatures in the thermal cycle the warpage of the package could be characterized as shown in Figure 4-17.

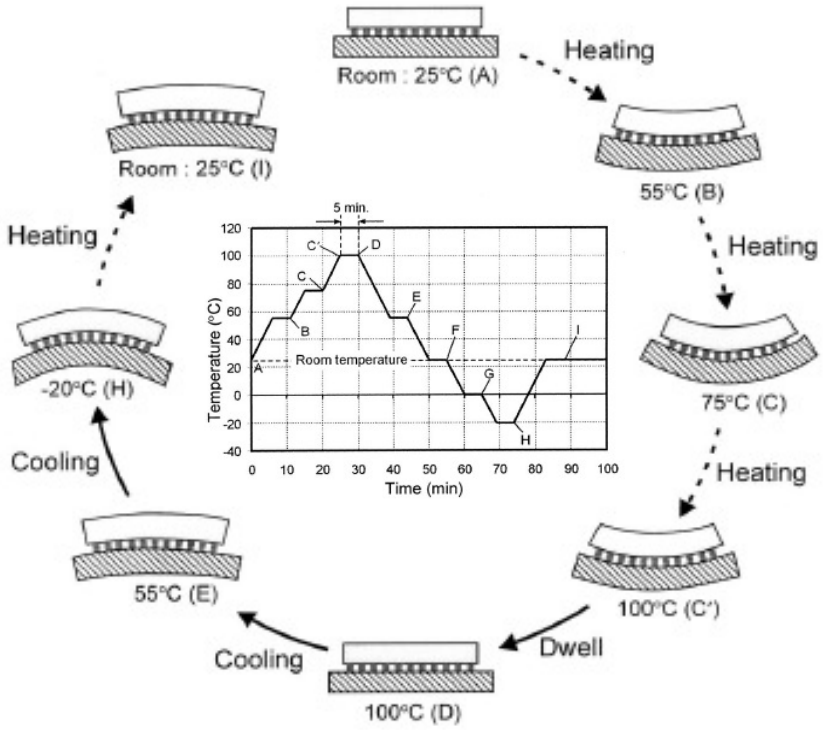


Figure 4-17. Schematic illustration of the deformation of the CBGA package assembly during the thermal cycle [108]

Significant relaxation can be seen at 100°C due to creep and the dwell time at time *D*. Upon cooling down to -20°C the curvature reverses, creep is suppressed, and the plastic deformation is significant such that residual plastic deformation remains when room temperature is reached at point *I*.

An earlier study by Han [107] on CCGAs showed how the characteristic S-shape of a failed solder column occurs in a thermal cycle. While Han's study used a cast CCGA column that only has one fillet on the board side, the deformation of the CLASP structure is similar in principle.

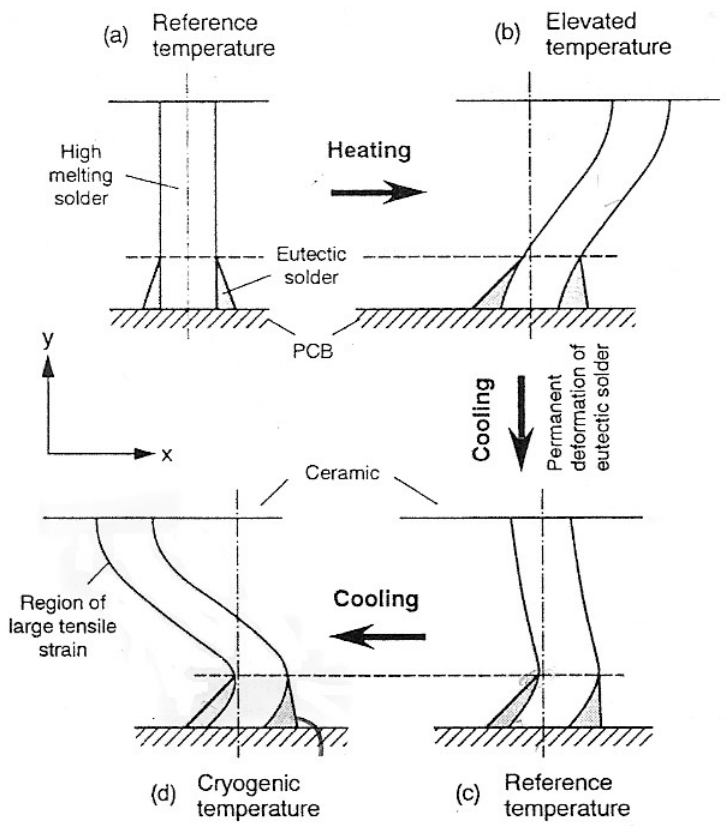


Figure 4-18. Schematic illustration of the deformation mechanism of a CCGA column during thermal cycling [107].

The 63Sn37Pb fillets have lower melting point than the 90Pb10Sn solder column. At high temperatures, the fillet allows the 90PB10Sn column to deform. As the temperature lowers, the 63Sn37Pb fillets hard and constrain the 90Pb10Sn. As the temperature continues to lower, the 90Pb10Sn is forced to bend around the 63Sn37Pb fillet and high strains develop at the intersection of the 63Sn37Pb fillets and 90Pb10Sn column. Failure will occur in the 90Pb10Sn due to the high strains at the stress concentration and bending mode included by the CTE mismatch between the ceramic substrate and FR4 board.

4.6. VIBRATION THEORY

A simple review of vibration theory for single degree of freedom (SDOF) harmonic vibration systems will be given in order to highlight the key concepts and equations used to characterize the CCGA system under harmonic out-of-plane vibrations. Once the

fundamentals of a SDOF system are laid out, then solving for multi-degree of freedom (MDOF) systems is done by assembling the equations of motion into matrix form and performing an eigenvalue and eigenvector analysis.

In addition, an analytical model based on Power Law formulation and Rayleigh-Ritz method for a continuous beam is used to determine the fundamental frequency and modes shapes of the CCGA test vehicle. The analytical equation will be used to estimate the fundamental frequency of the CCGA test vehicle and examine how the stiffness of the interconnect and mass of the heat sink affect the fundamental frequency of the system.

For further details, the reader is referred to the textbooks by Thomson [109] for derivation of the SDOF equations and to Ginsberg[110] for the details to develop the analytical model for the CCGA experimental test vehicle.

4.6.1. SDOF

The spring-mass-damper system of Figure 4-19 constitutes a damped SDOF system under a harmonic excitation force. The displacement coordinate x of the mass is known as a generalized coordinate and is used to describe the motion of the system. The generalized coordinate x can be described as $x=L-l_0$, where l_0 is the original length of the spring at rest and L is the current length of the spring.

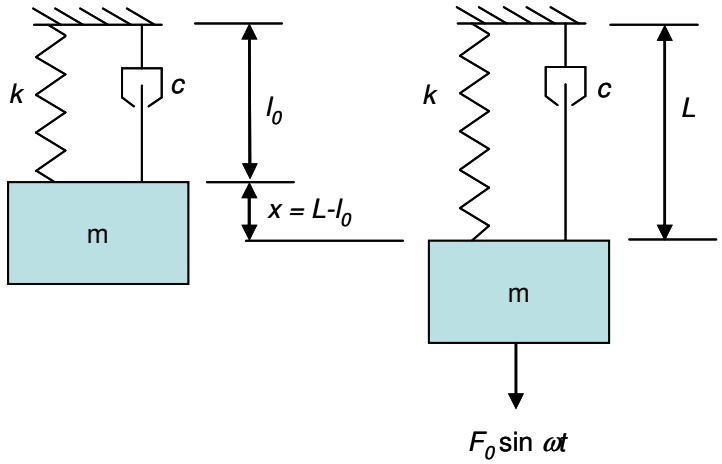


Figure 4-19. SDOF system under harmonic excitation.

The force balance equation of the spring, mass, damper system shown in Figure 4-19 results in the equation of motion:

$$m\ddot{x} + c\dot{x} + kx = F_0 \sin \omega t \tag{4.16}$$

where m is the mass of the system, c is the damping constant of proportionality, k is the spring constant, F_0 is the amplitude of the excitation force, and ω is the excitation frequency in rad/s.

The particular solution of Eq. (4.16) is a steady-state oscillation in the form of

$$x = X \sin(\omega t - \phi) \tag{4.17}$$

where X is the amplitude of oscillation and ϕ is the phase of the displacement relative to the excitation force.

Substitution of Eq. (4.17) into differential Eq. (4.16) and rearrangement to solve for the displacement amplitude X and the phase angle ϕ in nondimensional forms lead to

$$X = \frac{F_0 / k}{\sqrt{\left(1 - \frac{m\omega^2}{k}\right)^2 + \left(\frac{c\omega}{k}\right)^2}} \tag{4.18}$$

and

$$\phi = \tan^{-1} \frac{c\omega / k}{1 - m\omega^2 / k} \tag{4.19}$$

The following defined quantities can be substituted into Eqs. (4.18) and (4.19):

$$\omega_n = \sqrt{\frac{k}{m}} = \text{undamped natural frequency} \tag{4.20}$$

$$r = \frac{\omega}{\omega_n} = \text{frequency ratio} \tag{4.21}$$

$$c_c = 2m\omega_n = \text{critical damping} \tag{4.22}$$

$$\zeta = \frac{c}{c_c} = \text{damping ratio} \tag{4.23}$$

The nondimensional forms of Eqs. (4.18) and (4.19) with the above defined quantities results in

$$\frac{Xk}{F_0} = \frac{1}{1 + 2i\zeta r - r^2} \tag{4.24}$$

and

$$\phi = \tan^{-1} \frac{2\zeta r}{1 - r^2} \tag{4.25}$$

Equations (4.24) and (4.25) show that the nondimensional amplitude X_k/F_0 and the phase angle ϕ are functions of the frequency ratio r and the damping ratio ζ as shown in Figure 4-20.

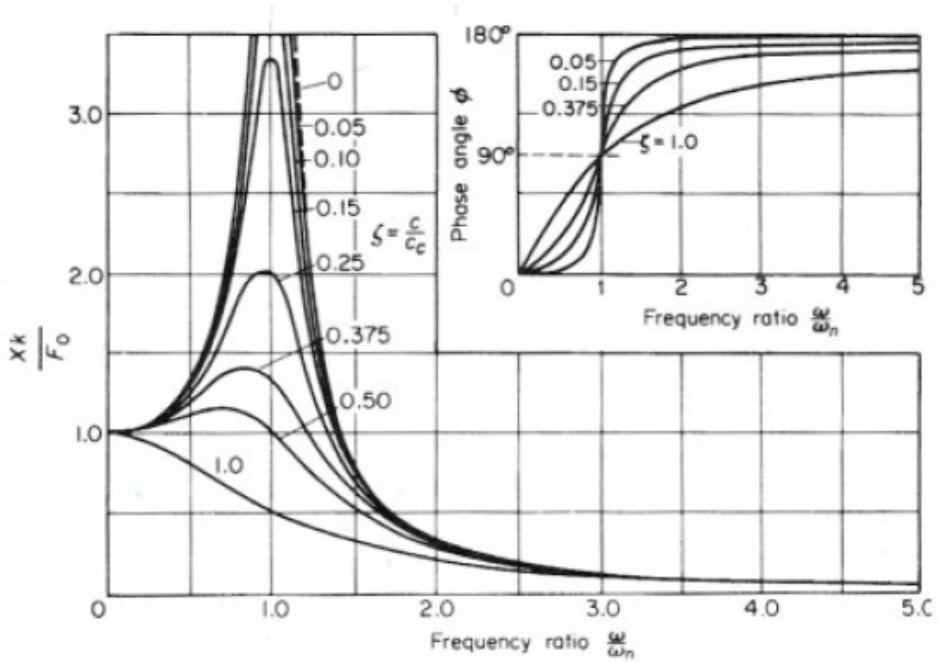


Figure 4-20. Nondimensional amplitude Eq. (4.24) and phase angle Eq. (4.25) for a harmonic SDOF.[109]

From Figure 4-20 it can be seen that the below r <1 the amplitude is close to 1, as the frequency ratio approaches r=1 (known as resonance) the amplitude increases drastically for damping ratios ζ<0.10, and at frequency ratios r >>1 the amplitude is less than 1. The phase angle at r=1 becomes 90^0 which may be interpreted as the inertial force $m\omega^2 X$ being balanced by the spring force kX, and the excitation force F_0 overcoming the damping force $c\omega X$. Experimentally, the fundamental frequency ω_n of a system can be found by sweeping the excitation frequency ω until the displacement x reaches a maximum and lags the excitation force by approximately 90^0.

In reliability testing, it is especially important to know a system's fundamental frequency ω_n in order to avoid having any external excitations in the environment sweeping through resonance or residing near it. In order to avoid resonance, the natural frequency of the system is often changed as it is usually not feasible to change the frequencies of the environmental forces that act upon the system. As seen from Eq. (4.20) the natural frequency ωn can be changed by either increasing the system's stiffness k or by decreasing the mass m of the system. Typically, stiffeners are added to the PCB board in order to increase the stiffness of the system. Additionally, the amplitude at resonance can be significantly lowered by increasing the damping ratio ζ with rubber mounts or snubbers. Caution should be used with this approach as damping material breaks down with time and can severely impact the performance of the system [55].

4.6.2. MDOF

The SDOF of Figure 4-19 has only one degree of freedom and correspondingly one natural frequency, called the fundamental frequency. A system with *N* degrees of freedom will have *N* corresponding natural frequencies. Each natural frequency will have a corresponding normal mode shape. The natural frequencies and mode shapes can be found by an eigenvalue and eigenvector analysis. The equations of motion in matrix form is

$$[M]\{\ddot{q}\}+[C]\{\dot{q}\}+[K]\{q\}=[F_0] \tag{4.26}$$

where $\{q\}$ is the vector of generalized coordinates.

For harmonic motion, the generalized coordinates $\{q\}$ can be written in complex notation:

$$\{q\}=\mathrm{Re}\left[B\{\phi\}\exp(i\omega t)\right] \tag{4.27}$$

where *B* and $\{\phi\}$ are constants.

The natural frequencies ω_j and corresponding mode shapes are solved by setting [C]=0 and [F_0]=0, substituting Eq. (4.27) into Eq. (4.26), and solving the eigenvalue problem of Eq. (4.28)

$$\left|[K]-\omega^2[M]\right|\{\phi\}=\{0\} \tag{4.28}$$

4.6.3. Analytical Equation to model CCGA test setup

An analytical model based on the Power Balance law is used to determine the natural frequencies and mode shapes, and to examine the influence of the geometry parameters on the natural frequency and mode shapes of the system. In this work, the solder joints are treated as individual stiffness elements and this work is capable of predicting natural frequencies and mode shapes for a variety of boundary conditions and component configurations. The analysis presented here assumes that a CCGA package with uniform mass m is attached to a printed circuit FR4 board through solder columns and that the FR4 board is clamped on both ends. For the sake of simplicity, a two-dimensional model as shown in Figure 4-21 is considered.

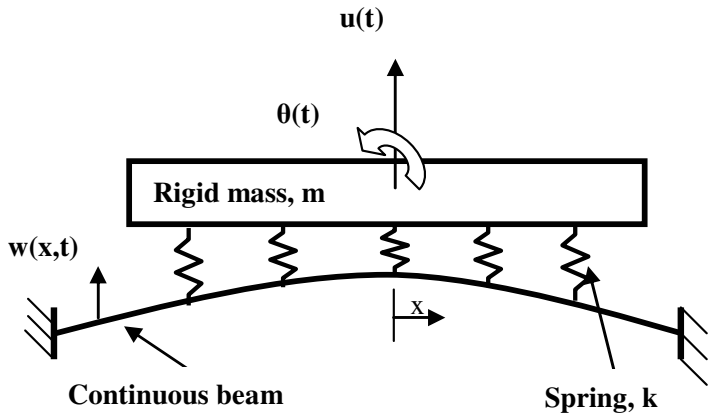


Figure 4-21. Schematic for analytical model of CCGA on FR4 board

For a conservative system with no external work, the general work energy principle in Eq. (4.29) states that the change of rate of kinetic energy (T) plus the change of rate of the potential energy (V) is equal to the zero

$$\dot{T} + \dot{V} = 0 \tag{4.29}$$

The FR4 board is modeled as a continuous beam using an N term Ritz series for flexural motion:

$$w(x,t) = \sum_{j=1}^{N} \psi_j(x) q_j(t) \tag{4.30}$$

where $\psi_j(x)$ is a kinematically admissible basis functions, and is

$$\left(\frac{x}{L}\right)\left(1-\frac{x}{L}\right)\sin\left(\frac{j\pi x}{L}\right)$$

for a fixed-fixed beam, and $q_j(t)$ are the unknown generalized coordinates of the beam.

Convergence for the analytical model up to the 2nd natural frequency was found with 10 Ritz series terms which act as the generalized coordinates of the beam.

The solder joints are modeled as discrete axial springs with spring stiffness, k=1200 N/mm, determined from finite element modeling. Because this is a 2D model and the out of plane stiffness needs to be accounted for properly, the spring stiffness k is multiplied by the number of springs (33) in the width of the CCGA. The CCGA package is modeled as a rigid mass m with a vertical degree of freedom $u(t)$ and a rotation degree of freedom $\theta(t)$ about the center of gravity. It is valid to treat the ceramic substrate as rigid due to its high stiffness; however this assumption will not be valid for plastic packages. The total degrees of freedom for the system will be N+2.

The kinetic energy of the system is

$$T = \frac{1}{2}\int_0^L \dot{w}^2 \rho A dx + \frac{1}{2} m \dot{u}^2 \tag{4.31}$$

where, L is the length of the FR4 board, ρ is the density of the FR4 board, A is the cross-sectional area of the FR4 board, m is the mass of the CCGA package, and u is the displacement of the CCGA mass m.

The potential energy is shown in equation (4.32)

$$V = \frac{1}{2}\int_0^L EI\left(\frac{\partial^2 w}{\partial x^2}\right)^2 dx + \frac{1}{2}\sum_{i=1}^{\#springs} k[(u + x_k\theta) - w(x_k,t)]^2 \qquad (4.32)$$

where, x_k is the position of spring relative to center of CCGA, and $w(x_i,t)$ is the beam displacement at location x of the ith spring.

Matrix equations of motion can be derived by substituting the Ritz series Eq. (4.30) into Eqs. (4.31) and (4.32), and the mass matrix [M] derived from the kinetic energy, T, will be:

$$M_{j,n} = \int_0^L \psi_j \psi_n \rho A dx + m\psi_j(x_m)\psi_n(x_m) \text{ for j, n} = 1 to \text{ N}$$

$$M_{N+1,N+1} = m$$

$$M_{N+2,N+2} = \text{mass moment inertia of block}$$

where, N+1= u degree of freedom, and N+2= θ degree of freedom.

Likewise, the stiffness matrix [K] derived from the potential energy, V, will be:

$$K_{j,n} = EI\int_0^L \frac{\partial^2\psi_j}{\partial x^2}\frac{\partial^2\psi_n}{\partial x^2}dx + \sum^{\#springs} k\psi_j(x_k)\psi_n(x_k) \text{ for j, n} = 1 \text{ to N}$$

$$K_{N+1,N+1} = \sum k$$

$$K_{N+1,n} = -k\sum \psi_n(x_k)$$

$$K_{N+1,N+2} = k\sum x_k$$

$$K_{N+2,n} = -k\sum \psi_n(x_k)x_k$$

$$K_{N+2,N+2} = k\sum x_k^2$$

where, N+1= u degree of freedom, and N+2= θ degree of freedom

The system now looks like a familiar discrete system of Eq. (4.26) and the eigenvalue problem of Eq. (4.33) can be solved for the N+2 natural frequencies and mode shapes.

$$[[K] - \omega^2[M]]\{\varphi\} = 0 \qquad (4.33)$$

where, ω is the frequency in rad/s, and φ is the mode shape vector.

The reader is referred to Ginsberg [16] for additional details on developing and solving Eq. (4.33).

Figure 4-22 shows the first two mode shapes predicted by the analytical method. Only the FR4 board is shown in Figure 4-22.

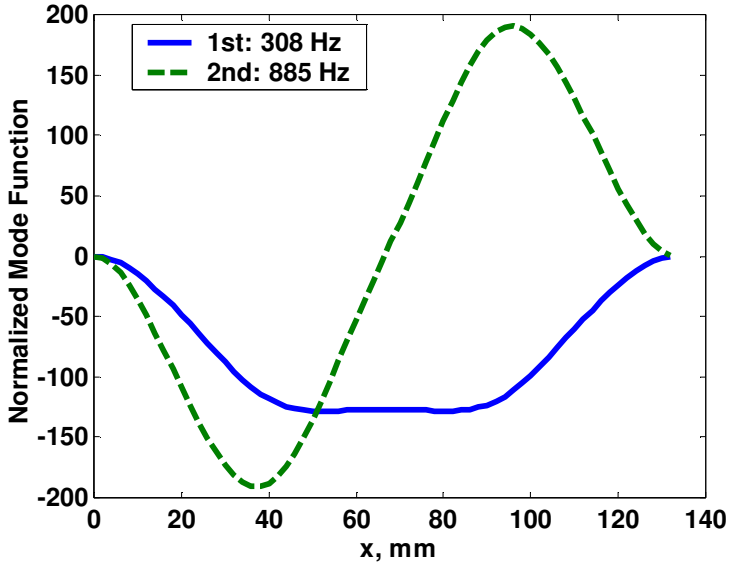


Figure 4-22. Mode Shapes from analytical method for FR4 with a 1089 I/O CCGA.

From Figure 4-22 it can be seen that the fundamental frequency is 308Hz. This estimate of the fundamental frequency will provide as a guide in the experimental test.

Due to its 2D nature, the analytical model cannot predict all mode shapes. Thus, we will only use it to look at characteristics of the first natural frequency with the analytical method. It is also observed that the analytical model over predicts the natural frequencies because the solder joints are modeled as single springs with no rotational motion. However, the analytical model is still useful for quick qualitative analysis.

4.6.4. Effect of Interconnect Stiffness on Mode Shape of Board

The stiffness of the interconnect will change depending on the standoff height, cross-sectional area, and the material used for interconnect. For example, if copper columns are used instead of 90Pb10Sn solder columns, the stiffness will be 11000 N/mm. It is seen in Figure 4-23 that the curvature of the board is quickly reduced as the stiffness

increases. Modeling the solder joints as one spring will not capture the local stiffening effect.

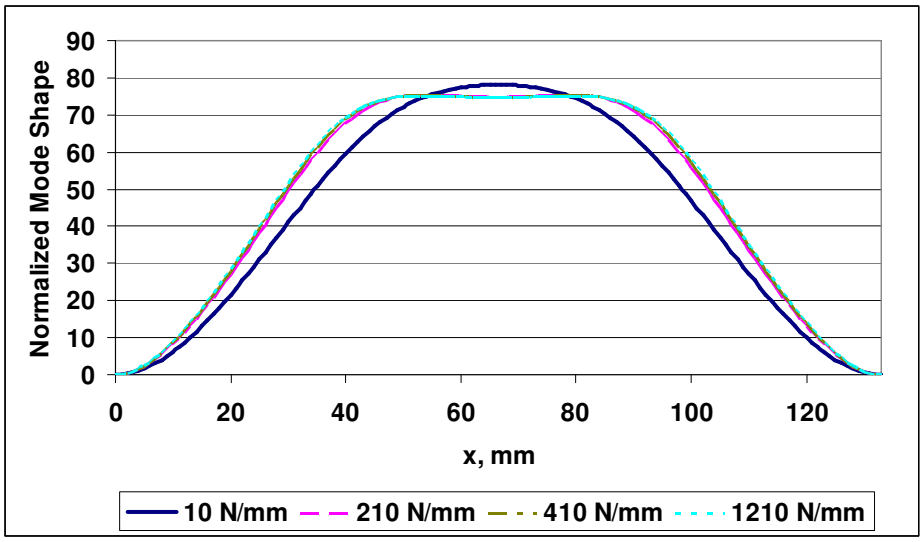


Figure 4-23. Effect of Stiffness on First Mode Shape

4.6.5. Effect of Interconnect Stiffness and Component Mass on the Fundamental Frequency

Table 4-3 plots natural frequency as the stiffness approaches 1000 N/mm for a range of heat sinks from 0 to 0.150 kg attached to the CCGA package.

Table 4-3. Effect of Interconnect Stiffness and Heat Sink Mass on Fundamental Frequency

	Mass of heat sink			
Stiffness (N/mm)	0 kg	0.05 kg	0.10 kg	0.15 kg
10	269	190	155	134
200	320	229	187	162
400	329	236	193	168
1000	340	243	200	174
1200	342	245	201	175

Table 4-3 shows that increasing the stiffness of the interconnects beyond 400 N/mm does not change the characteristics of the system significantly. On the other hand, increasing the heat sink mass will decrease the natural frequency of the system.

A CCGA ceramic package is much heavier compared to other packages such as flip chip or CSP. Adding a heat sink onto the CCGA can increase inertial forces significantly and accelerate failure [19]. Cole at al. from IBM Corp. recommend a maximum heat sink mass of 132g for a 42.5mm square CCGA with 1089 interconnects [20].

4.7. CHAPTER SUMMARY

The background material presented in this chapter is sufficient to understand the fundamentals of solder joint reliability for CBGA and CCGA electronic packages. The CBGA and CCGA packages structure was introduced, the fundamentals of solder joint material behavior and modeling was covered, laser moire interferometry specifically for CBGA and CCGA was introduced, and the fundamentals of harmonic vibration analysis was introduced. The next chapter will develop the unified finite element modeling methodology for predicting solder joint fatigue under thermal cycling, power cycling, and vibration environments.

CHAPTER 5

UNIFIED FINITE ELEMENT MODELING METHODOLOGY FOR PREDICTION OF SOLDER JOINT FATIGUE UNDER THERMAL. POWER, AND VIBRATION ENVIRONMENTS FOR CERAMIC AREA ARRAY ELECTRONIC PACKAGES

5.1. INTRODUCTION

Separate FEMs are typically constructed for each loading environment due to variations in element types and capabilities for each environment. Calculation and comparison of damage parameters may be inconsistent between models as mesh, boundary conditions, and element types change between models. A single FEM for all environments will enable calculation of damage under each environment. Therefore, this chapter aims to develop a unified FEM for predicting solder joint fatigue of a Ceramic Column Grid Array (CCGA) under thermal, power cycling, and vibration modeling.

Alongside with the CCGA FEM development, a unified FEM for CBGA will be developed using the same techniques, however only the thermal-mechanical and power cycling environments will be validated. The vibration environment is not considered for CBGA because vibration experiments were not performed on CBGA.

The developed CCGA and CBGA FEMs will be validated with experimental data in chapter 6 for ATC and PC environments, and chapter 7 for vibration environments.

5.2. UNIFIED FINITE ELEMENT MODELING METHODOLOGY

The objective is to develop a single, unified modeling methodology capable of capturing damage in the solder joints under thermal cycling, power cycling, and vibration environments. The requirements for developing such a unified modeling methodology for large area array electronic packages are:

- The modeling methodology should be able to accommodate the loading induced by thermal cycling and power cycling as well as vibration.
- The modeling methodology should be able to determine thermal gradients associated with power cycling and at the same time, should facilitate the determination of fundamental frequencies and mode shapes associated with vibration loading.
- The modeling methodology should facilitate detailed solder geometry modeling necessary for low cycle fatigue failure and at the same time, should allow for simplification of non-critical solder joints to obtain vibration parameters. Representing the structural and thermal contribution of every solder joint is critical.
- As the modeling methodology needs to accommodate different type of loading conditions, symmetry and other assumptions should be carefully addressed in the model to ensure that the results are accurate.
- The modeling methodology should facilitate appropriate material behavior (elastic-plastic-viscoplastic) to account for solder deformation mechanism under thermal cycling, power cycling, and vibration loading conditions.
- The modeling methodology should be able to determine the accumulated damage metric induced by low-cycle thermal cycling and power cycling loading conditions as well as high-cycle vibration loading conditions.
- As the unified finite-element model is three-dimensional in nature, the modeling methodology should have facilities to account for a combination of coarse-fine finite element mesh, equivalent-beam and detailed model, and elastic-plastic and viscoplastic material model.

- The modeling methodology must keep a consistent finite element mesh when solving for thermal cycling, power cycling, and vibration loading environments. This involves matching element types with appropriate material models and solution capabilities. Many finite element programs have restrictions on which material models can be used with certain elements. This makes it difficult to use consistent material properties and mesh across all three environments.

A 3D FEM, shown in Figure 5-1 for CCGA and Figure 5-2 for CBGA, was developed in ANSYS 9.0™ [111] using solid and beam elements to calculate a damage parameter. Quarter symmetry is used for thermal and power cycling, and a full 3D model is used for vibration modeling in order to capture all mode shapes. Computational efficiency and accuracy are maintained by using an equivalent beam approach which entails representing the solder joints that are not of primary interest with equivalent beams that effectively capture the global axial stresses, shear stresses, moments, time-dependent creep behavior, and thermal resistance of a finely detailed joint. The equivalent beam method has gained recent popularity [11, 13, 112, 113] due to its efficiency and accuracy at simulating a full array of solder joints. The enhanced equivalent beam method used in this study is the first to include creep and thermal properties in the equivalent beam approach.

It should be noted that if underfill is used then there may not be a need for the equivalent beam method as a layer with properties equivalent to the composite solder/underfill structure could be developed.

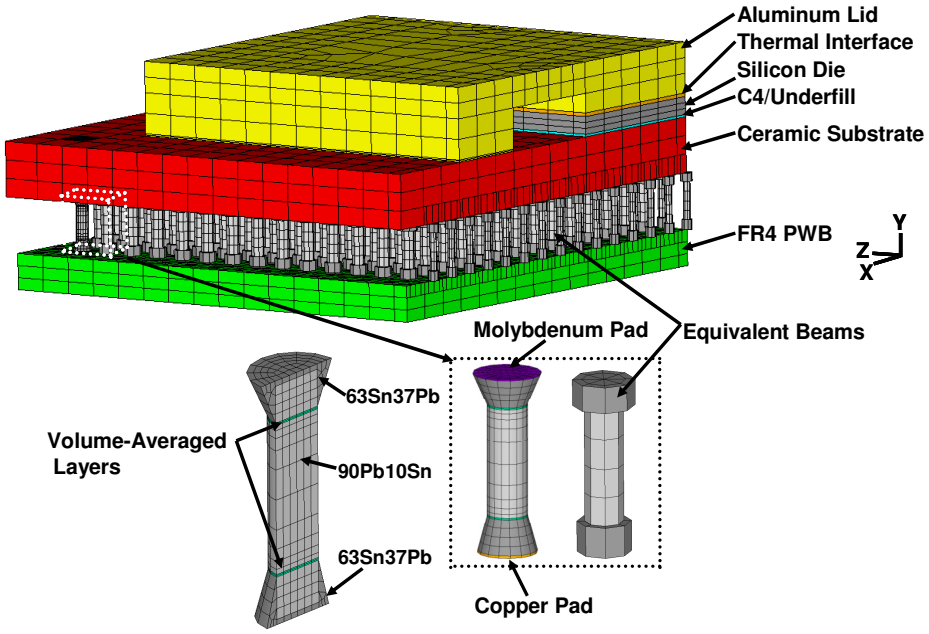


Figure 5-1. 3D quarter FEM with solid detailed joint and equivalent beam for CCGA

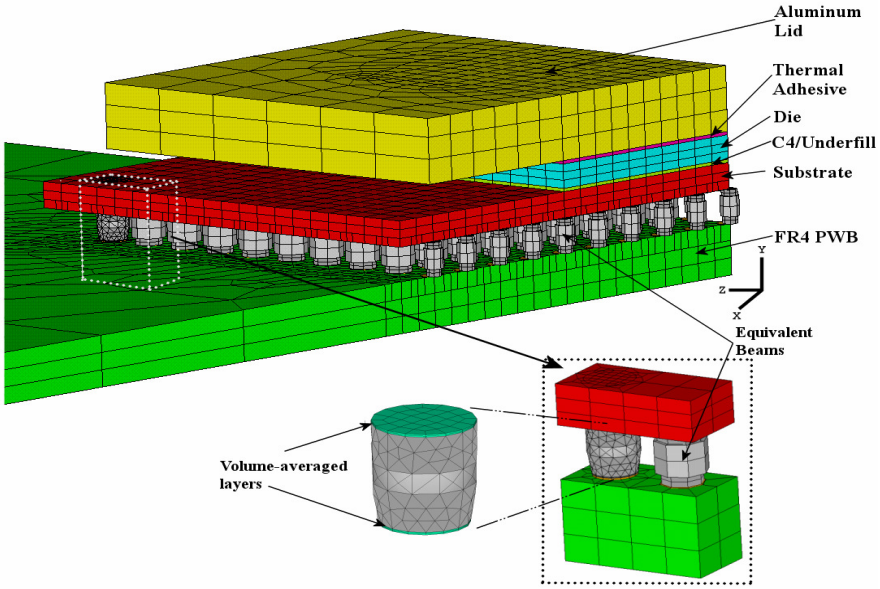


Figure 5-2. 3D quarter FEM with solid detailed joint and equivalent beams for CBGA

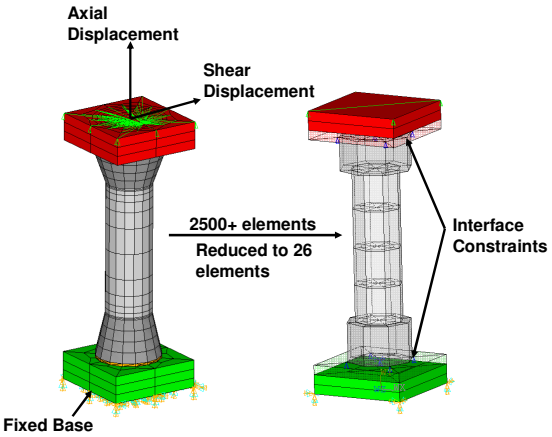
The method to develop the equivalent beams will now be discussed in detail in the next section.

5.2.1. Equivalent Beam Modeling

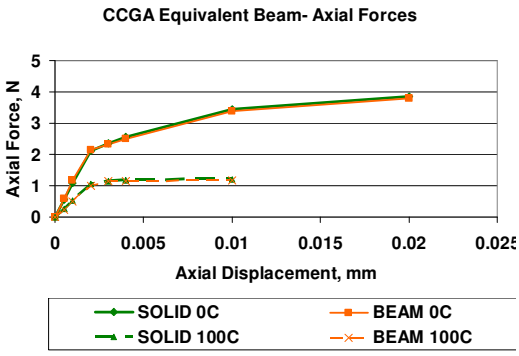
The objective is to develop an equivalent beam model that can capture the global force/moments and relaxation of a solder joint to model solder joints not of primary interest. It should be noted that this equivalent beam approach is similar to that of Corbin [13]. Corbin performs a global/local modeling analysis where displacements from the global model are applied to a local model of the solder joint. However, the approach in this paper avoids a global/local approach by directly incorporating a solder joint model into the global model.

The equivalent beam model must reproduce the same axial (Y axis) forces as the local model when uniform displacements in the Y direction are applied to the top of the substrate. In addition, the equivalent beam must also produce similar shear (X/Z axis) forces and moments when uniform shear displacements in the X/Z direction are applied to the top surface. The applied displacements are representative of the actual displacements that different solder joints would experience under thermal cycling, and also, are sufficiently high to introduce both the elastic and the inelastic deformation in the solder joint. The geometry and the material properties of the beams are determined iteratively in the plastic region.

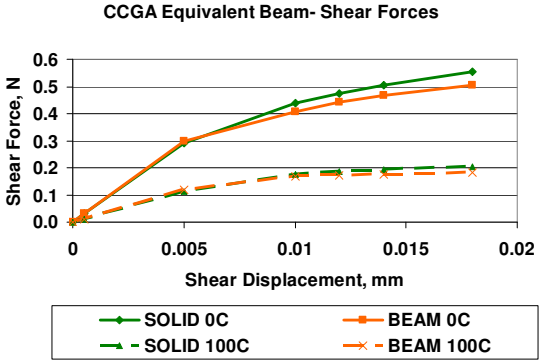
The detailed SOLID joints shown in Figure 5-3a and Figure 5-4a consist of SOLID quadratic elements to model the 90Pb10Sn ball and 63Sn37Pb fillets. The molybdenum pad, copper pad, and board and substrate are modeled using solid linear elements. The PWB and substrate are modeled to ensure the interface behavior between the joint and respective PWB/substrate is captured correctly. The thickness of the PWB and substrate is limited to 0.3mm so as not to overwhelm the behavior of the joint during the characterization process. The base of the PWB is constrained in all directions and the top surface of the substrate is coupled in the vertical direction as illustrated in Figure 5-3a and Figure 5-4a.



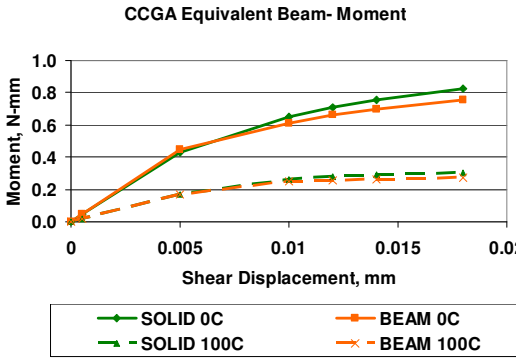
a) Detailed Model and Equivalent Beam



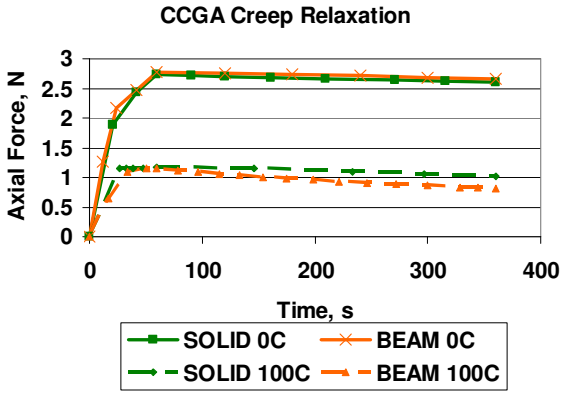
b) Axial Force Equivalence. 3% average error



c) Shear Force Equivalence. 7% average error



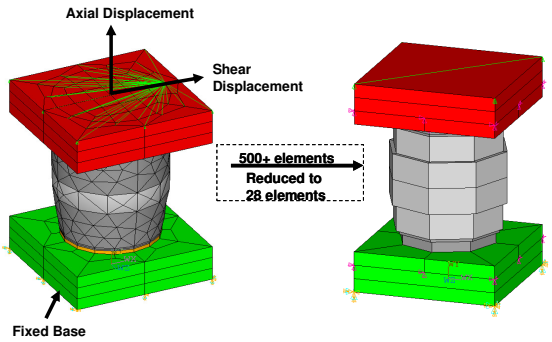
d) Moment Equivalence. 7% average error



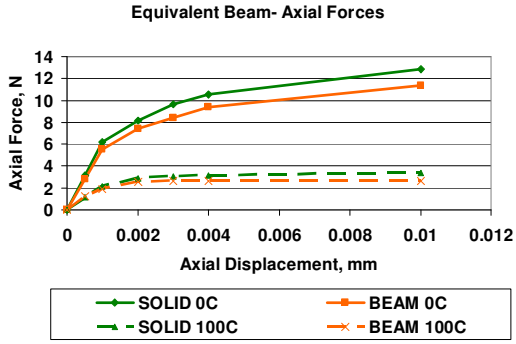
e) Creep Equivalence. 5% average error.

Figure 5-3. Equivalent Beam Model for 1.27mm pitch CCGA.

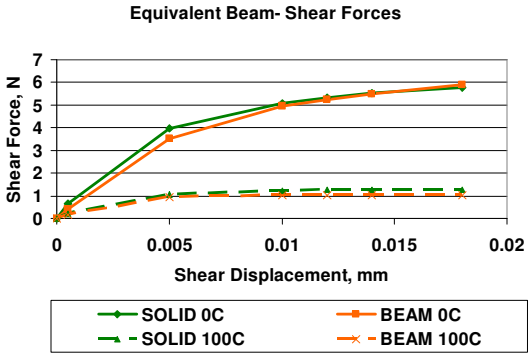
The equivalent beam model for a CBGA on 1.27mm pitch is given in Figure 5-4.



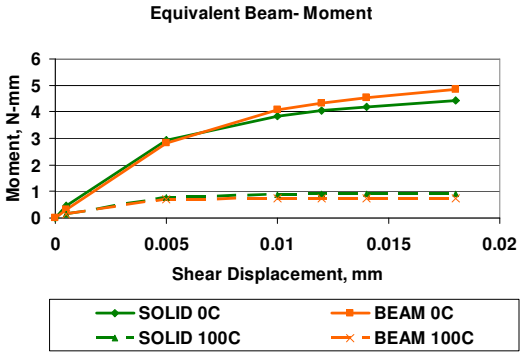
a) Detailed Model and Equivalent Beam



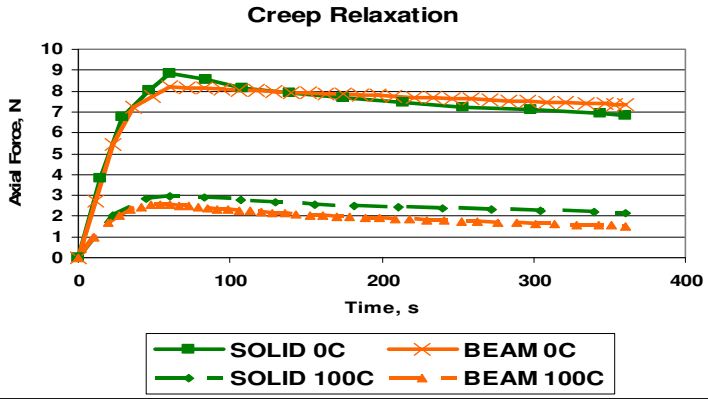
b) Axial Force Equivalence. 11% average error



c) Shear Force Equivalence. 12% average error



d) Moment Equivalence. 15% average error



e) Creep Equivalence. 12% average error.

Figure 5-4. Equivalent Beam Model for 1.27mm pitch CBGA.

The equivalent beam joint shown in Figure 5-3a and Figure 5-4a consists of six beam elements and the equivalent behavior is determined by varying the lengths and radius' of

the beams. The material properties of the beam are the same as the detailed solid joint. Modeling the interface between the beam elements of the joint and solid elements of board and substrate is critical. Two factors must be considered: 1) The beam element has a rotational degree of freedom that the solid elements lack. Therefore the rotational degree of freedom in the beam element must be constrained in order to prevent the beam from being free to rotate like a ball joint; and 2) The beam element applies forces, moments, and heat flow only at a point which will unrealistically distort/overheat the board and substrate interfaces. In a real joint, the forces/moments, and heat flow are distributed over the pad area.

These two difficulties can be overcome by using appropriate constraint equations at the interfaces which act to: 1) constrain the beam rotational degree of freedom by tying it to the vertical displacements of the interfaces, and 2) distribute the point force/moment/heat flow over an area equal to the pad areas.

Determining the geometry of the beam element involves an iterative process of balancing the axial and shear responses. Axial displacements are applied to the top surface of the substrate and the reaction force of the top surface is measured. The axial displacements are large enough to enter the plastic region. The length and radii of the beams are changed until the average error of the axial reaction force between the detailed and equivalent beam model is under 15%. Next, shear displacements are applied to the top surface of the substrate and the shear reaction force and moment at the top surface is measured. The length and radius of the beams are changed until the average error of the shear reaction force and moment are under 15%. Next, the axial displacements are again applied and the geometry changed until the average error is under 15%. The iterative process continues until a combination of lengths and radius' of the beams allows for less than 15% error in axial forces, shear forces, and shear moments. Finally, the creep behavior of the equivalent joint is verified by applying an axial displacement and holding

it while recording the force relaxation. The procedure is performed at 0°C and 100°C to capture temperature dependent behavior. The procedure is performed each time the solder joint geometry is different, such as the case when a smaller diameter is used for the 1.00mm CBGA. The final characterization of the equivalent beam for Pb containing CCGA solder joints at 1.27mm pitch is shown in Figure 5-3b-e. The analysis is repeated anytime the solder joint geometry changes, such as when the pitch is 1.00mm and the pad sizes change.

The equivalent beams must also be thermally equivalent to the local model for power cycling. This is accomplished by using linear, rectangular link elements (LINK33) with appropriate thermal conductivities and cross-sectional areas. Only 1D conduction is considered. Radiation and convection on the joints is neglected.

5.2.2. Boundary Conditions

Boundary conditions for the ATC and PC 3D quarter model consist of constraining the out-of-plane displacements/rotations of the symmetry planes to zero and constraining one point completely at the intersection of the symmetry planes as shown in

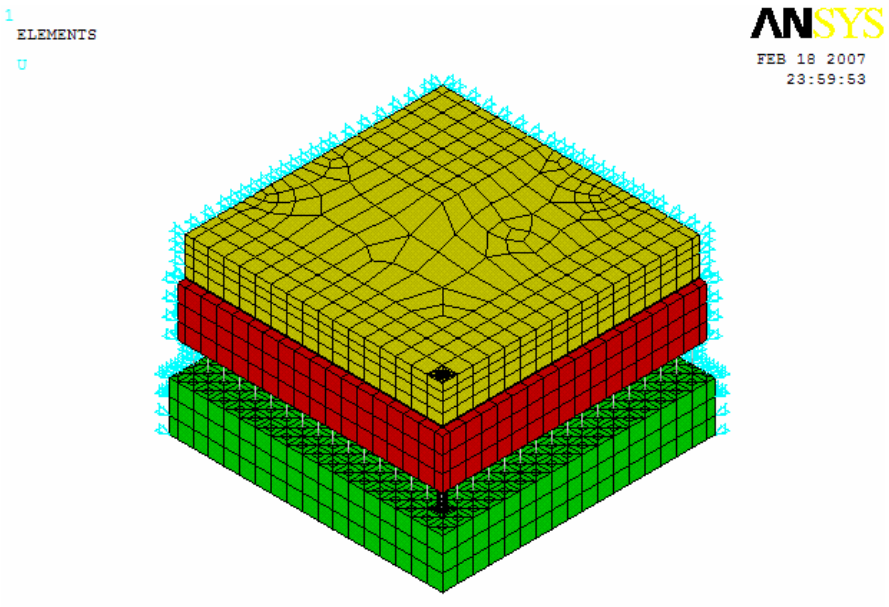


Figure 5-5. 3D quarter FEM of CCGA with boundary conditions

Additional boundary conditions for the PC 3D quarter model consist of constraining the symmetry planes to be adiabatic, applying a heat flux to the bottom surface of the die which is active, and applying appropriate constant convection coefficients to exposed surfaces. For forced airflows of 0.5 m/s, 1.0 m/s, and 2.0m/s the constant convective coefficients using boundary layer flat plat laminar flow theory are 14.9 W/m^2K, 21.1 W/m^2K, and 28.9 W/m^2K [114] respectively are applied to top surfaces of the substrate and die (if exposed), and to the top and bottom surfaces of the PWB. A natural convection coefficient of 5 W/m^2K is applied to the vertical sides of the PWB, substrate, and lid. The bulk (ambient) temperature for all convections is 30^oC.

For the vibration modeling, the FEM of Figure 5-1 was expanded to a 3D full model that could capture the rigid body motion of the CCGA package assembly and all mode shapes. Unlike thermo-mechanical modeling where symmetry conditions are used to reduce computational time, in vibration models the entire assembly is modeled to be able to capture all of the vibration modes. In addition, it is important to ensure that masses are represented properly so that the inertial forces are correct. For this reason solid elements are used to model every mass. No point masses are used. Solid elements will also enable modeling of attached aluminum lids and heat sinks. The boundary conditions consist of constraining the ends of the board to be zero in all degrees of freedom as shown in Figure 5-6.

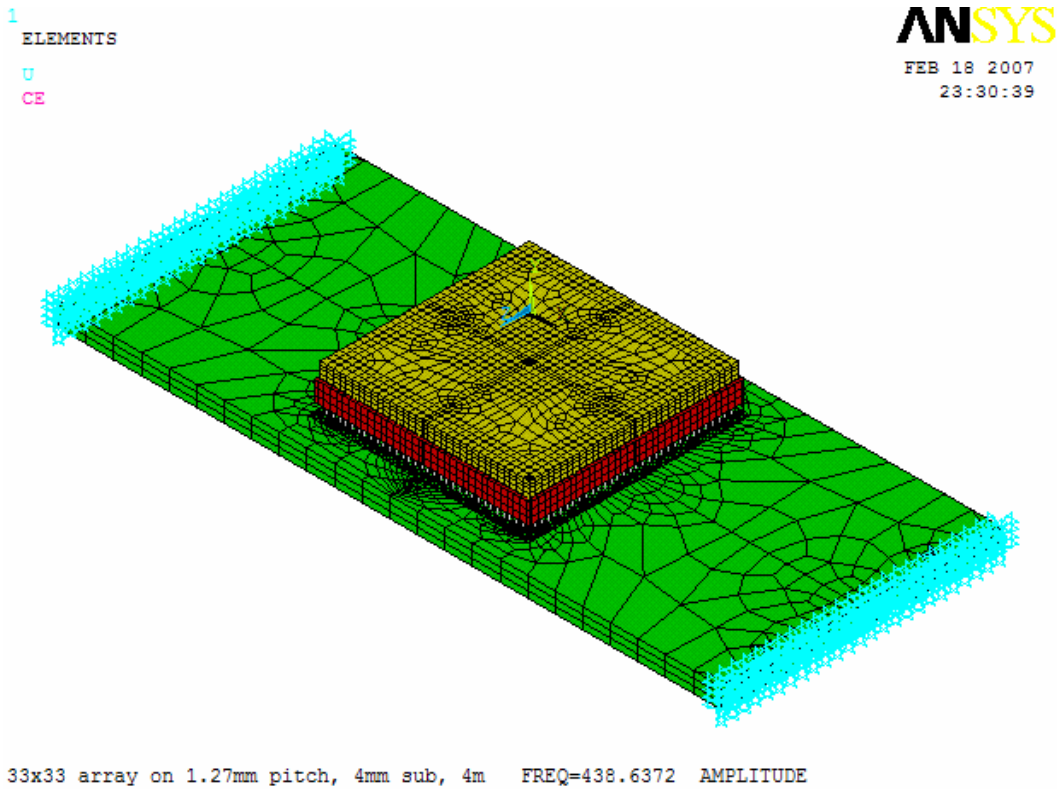


Figure 5-6. Full FEM of CCGA under vibration loading with constrained boundary conditions

5.2.3. Material Properties

Modeling the material properties of the solders is difficult because ANSYS only allows certain material models with certain elements. The overall goal is to have a consistent set of material properties and models no matter what element is used.

Linear material properties are given in Table 5-1 and the nonlinear temperature and time-dependent properties for the 63Sn37Pb and 90Pb10Sn solders are given in Table 5-2.

Table 5-1. Linear temperature independent material properties

Material	Young's Modulus (MPa)	Poisson's Ratio	CTE (ppm/K)	k (W/mm K)	C (J/tonne °C)	Density (tonne /mm^3)	Direction
FR4	27924-37K 12204-16K [115]	0.28 0.11	18.0 35.0	0.0121 0.00385	502E3	1.94E-9	(X,Z) (Y)
Alumina Ceramic	241E3	0.25	6.8	0.021	765E3	3.97E-9	

Material	Young's Modulus (MPa)	Poisson's Ratio	CTE (ppm/K)	k (W/mm K)	C (J/tonne °C)	Density (tonne /mm^3)	Direction
HICTE Ceramic	75E3	0.25	10.6*	0.002	765E3	3.97E-9	
Aluminum 6061T6	70E3	0.25	23.0	.240	963E3	2.7E-9	
Copper	123E3	0.34	17.0	0.389	385E3	8.96E-9	
Molybdenum	320E3	0.28	5.0	0.138	251E3	10.24e-9	
Silicon	130E3	0.30	2.62	0.117	712E3	2.33E-9	
C4/Ufill	14470	0.28	20.0	0.0006 0.0015	647E3	1.1E-9	(X,Z) (Y)
63Sn37Pb	plastic	0.4	21.6	0.036	170E3	8.4E-9	
90Pb10Sn	plastic	0.282	28.2	0.0519	184E3	10.8E-9	

*Measured according to [116]. Manufacturer lists at 12.3 ppm/K [117]

Table 5-2. Plasticity and Creep data for 63Sn37Pb and 90Pb10Sn solder

	Multi-Linear Kinematic Plasticity						Arrhenius Creep Model $\dot{\varepsilon} = C_7 \sigma^{C_8} \exp\left(\frac{-C_{10}}{T(K)}\right)$		
	Temp (K)	Strain 0.001	0.005	0.0075	0.01	0.06	C_7	C_8	C_{10}
90Pb10Sn (MPa)	273	10.34	16.05	17.36	18.12	26.70	0.15	4.0	7216.7
	323	9.41	10.95	12.00	12.54	16.24			
	373	5.62	5.80	5.90	6.01	6.76			
63Sn37Pb (MPa)	273	26.48	43.00	44.60	45.60	47.39	0.13	2.9	5172.0
	323	12.52	15.38	19.10	19.45	20.44			
	373	2.90	5.80	5.80	5.80	5.80			
SOURCE	[118]						Curve Fit using Garafalo model from [119]		

For vibration experiments where high strain rates ($\dot{\varepsilon} > 0.02s^{-1}$) are present, the yield stress is two to three times higher than the yield stress under thermo-mechanical loading [77]. Furthermore, when the frequency of loading is high and the time duration of testing is short (few minutes as opposed to hours and days), there is not enough time for creep strain to accumulate [81, 120]. Because of these reasons, the solder material is modeled as an elastic material with time-independent properties when vibration is the loading environment.

In order to model the solders under ATC and PC, the time-independent plasticity and the time-dependent creep properties of Table 5-2 must be put into proper material models

with compatible element types. The choice of material models and element types is described in the next section.

5.2.4. Choice of Material Models and Elements

The options for modeling the plasticity and creep of solder are described below.

5.2.4.1. Plasticity Models

Only multilinear models that allow for defining temperature dependent stress/strain curves with multiple points are considered. There are two common choices for modeling the plasticity of solder: multilinear kinematic hardening (MKIN) model is ideal as it includes the Bauschinger effect and is good for cyclic applications [121]; and multilinear isotropic hardening (MISO) which is not ideal for modeling solder in cyclic applications as it allows the yield surface to expand and after the first thermal cycle very little further plastic strain is accumulated [122].

5.2.4.2. Creep Models

ANSYS has two computational solution methods for creep and only certain material models can be used with each: explicit creep solves for the displacement from plasticity and then solves for the creep strain rate; implicit creep solves for the displacement by considering plasticity and creep simultaneously. Explicit creep takes a significant amount of computational time and is often unreasonable when modeling more than 10 solder joints. Implicit creep is the preferred method as it is computationally faster and more accurate.

Two common material models for creep behavior are; Garafalo/hyperbolic sinh equation is ideal as it covers the primary and secondary regions of the strain rate/stress curve well. ANSYS only allows the Garafalo model with an implicit creep solution; and the Norton power law equation is generally applicable when the stresses are not too high (< 35MPa). Since it is an exponential model, it will over predict creep strain rates at high stresses. The Norton power law is only available in an explicit solution method.

5.2.4.3. ANAND's Model

A common alternative to modeling creep and plasticity separately is to use Anand's model which is a unified viscoplastic law and is computationally very efficient. Anand's model will not be used in this study because: (1) BEAM188/189 elements do not allow for Anand's Model; (2) Anand's model is not allowed in a harmonic solution; and (3) the performance of the available Anand's model for 90Pb10Sn and 63Sn37Pb solders did not correlate to the separate plasticity and creep modeling.

5.2.4.4. Compatibility of Element Types and Material Models

Ideally, solder would be modeled with a MKIN/implicit combination of plasticity and creep, respectively, for accuracy and efficiency. However, as of ANSYS 10.0, there is no element type that will allow this combination. A combination of MISO/implicit is allowed, but as mentioned before it under predicts the plastic strain accumulation and is not good for predicting solder joint fatigue [122]. However, the MISO/implicit combination will be used in the equivalent beam elements where only displacement/forces are of concern. The local detailed joint will be modeled with the MKIN/explicit combination.

Solving for the damage in PC involves a two step solution in which the element types are changed. The first step is to solve for the transient thermal distribution when the die is powered on/off and convection is applied to the lid, substrate, and PWB surfaces. Appropriate thermal elements were used; linear, brick elements (SOLID70) were used for everything except in the thermally equivalent beam which are linear, rectangular link elements (LINK33). The second step involves switching from thermal to structural elements to solve for the displacements due to the temperature gradients: linear, brick elements (SOLID45) are used in the PWB, substrate, C4 flip chip/underfill layer, silicon die, thermal adhesive, and the direct lid attach (DLA); quadratic, brick elements (SOLID95/92) are used in the detailed solder joint; and linear, circular beam elements

(BEAM188) are used in the equivalent beams. The temperature solution from the transient thermal analysis is then read in as body loads on to the structural solution. To ensure that mesh dependency does not affect the results, the ATC and PC finite element models have identical meshes.

Table 5-3 gives the element and material model combinations used in this work.

Table 5-3. Compatibility for Element types and Material Models for solder

ANSYS Elements	Material models (plasticity/creep)	Purpose	Advantage	Disadvantage
BEAM188/189	*MISO/implicit*	Equivalent Beams	*implicit* creep solves quickly.	*MISO* not good for cyclic applications.
SOLID45/95	*MKIN/explicit*	Local joint for fatigue calculation	Properly models plastic and creep behavior of solder	Long computational time of *explicit* creep.
LINK33	--	Thermal modeling beams		

5.2.5. Calculation of Damage Parameter

A volume-weighted average is used to resolve the inherent problem of singularity in FEM when choosing which nodes/elements to take the damage parameter from. There are two 1mil thick layers of elements as shown in Figure 5-1 and Figure 5-2 in which the damage parameter per cycle Ψ is volume-averaged over. One layer is on the board side, and the other layer is at the substrate side. The layer with the highest volume-averaged damage parameter per cycle Ψ is used in Eq. (4.7). The layer with the highest damage parameter per cycle Ψ will change depending upon design parameters and environmental loading.

5.2.6. Choice of Stress Free temperature

In the FEM simulations, a temperature at which the model is stress-free must be chosen. The choice of stress free temperature will significantly affect the simulation time for each environment, especially when a factorial design of experiments is performed. The most

common choices for the stress free temperature in non-underfilled packages is either the reflow temperature of the solder, 183°C for 63Sn37Pb, or room temperature between 20°C and 25°C. The choice of the solder reflow temperature as the stress free temperature assumes that the model is stress free until the solder joints are attached and cooled, at which point residual stresses exist in the structure. The choice of room temperature as the stress free temperature assumes that all the stresses in the solder have relaxed after a significant amount of time when held at room temperature because solder is above 0.5 Tm at room temperature and creep can occur. It would be convenient for this study if 20°C could be used as the stress-free temperature so as to avoid the time of modeling a cool down from 183°C and long dwell at room temperature for each simulation. For this reason, the accuracy of choosing 20°C as the stress–free temperature over 183°C as the temperature distribution is investigated by comparing the total strain range per cycle, $\Delta\varepsilon_{tot}$, for each stress-free case.

A 25x25x2.9mm CCGA on 1.57mm FR4 with 1.27mm pitch was simulated for 3 cycles under 0/100°C 3cph with various stress free conditions: (1) 183°C with a 4 day hold at room temperature and (2) 20°C followed by temperature cycling with the high ramp first. Figure 5-7 plots the hysterisis loops for the stress and total strain components with 20°C as the stress free temperature. Similarly, Figure 5-8 plots the hysterisis loops for the stress and total strain components with 183°C as the stress free temperature.

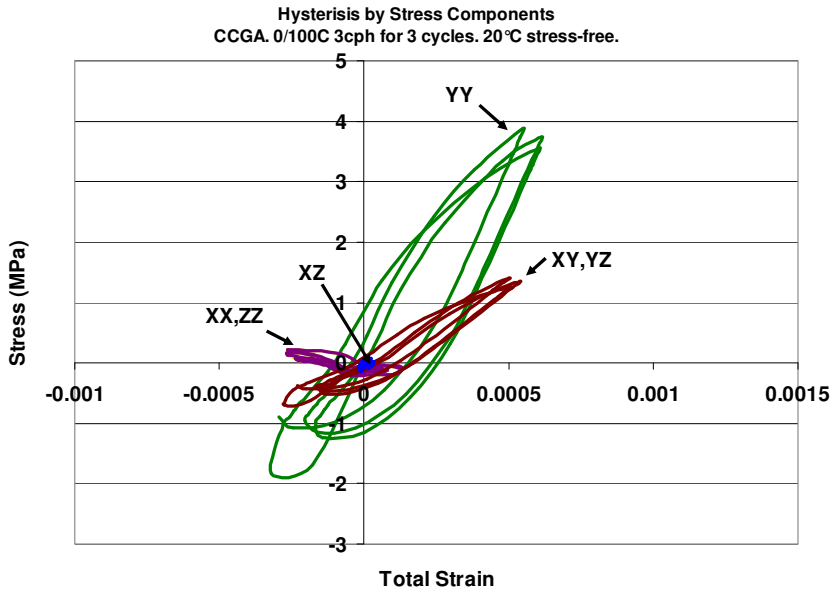


Figure 5-7. Hysterisis loops for CCGA with 20°C as stress-free temperature.

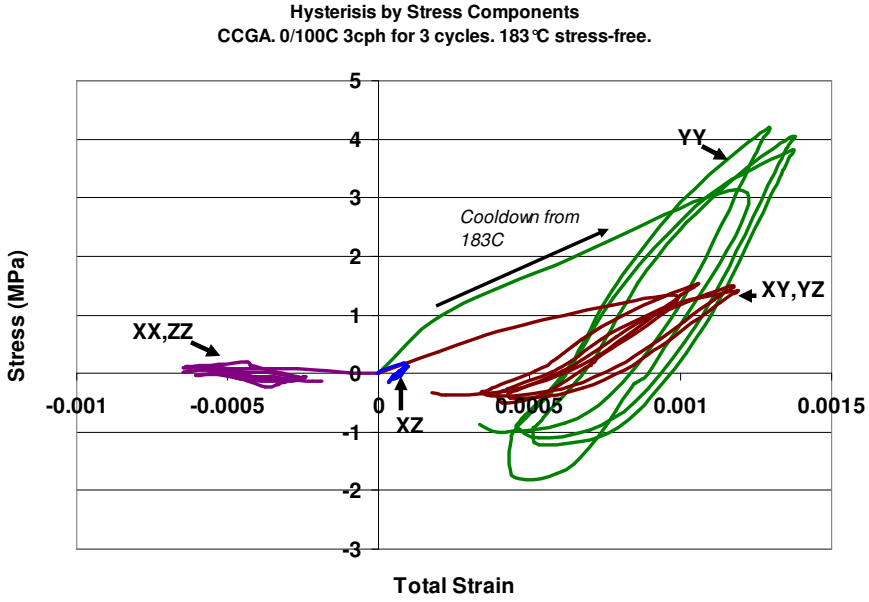


Figure 5-8. Hysterisis loops for CCGA with 183°C as stress-free temperature.

It can be seen from Figure 5-7 and Figure 5-8 that the stress range and total strain ranges are similar for each stress free temperature. The significant difference between a stress-free temperature of 183°C and 20°C is in the mean strain location of the axial stress (σ_{YY}) and the shear stresses (σ_{XY}, σ_{YZ}). The higher mean strain for 183°C as the stress-free temperature is due to the large deformation that occurs during the cool down from 183°C. After the 4 day dwell at room temperature, the stresses relax to nearly zero. Once

thermal cycling begins after the 4 day dwell at room temperature, the hysterisis loops looks similar to the case where 20°C is the stress-free temperature.

A damage parameter that may be used for fatigue life calculation is the total strain range per cycle, $\Delta\varepsilon_{tot}$. Table 5-4 shows the comparison of the total strain range per cycle and the mean total strain for the 183°C and 20°C stress-free temperature cases. The total strain range per cycle differs by less than 10% when 20°C instead of 183°C is the stress-free temperature. The mean total strain differs by 79% when 20°C instead of 183°C is chosen as the stress-free temperature. However, the mean strain is not taken into account when calculating the fatigue life. Therefore, 20°C is used as the stress-free temperature.

Table 5-4. CCGA Damage results from 3rd cycle.

Stress-free temperature	Total strain range per cycle,$\Delta\varepsilon_{tot}$	Mean total strain
183°C	0.00133	0.00198
20°C	0.00122	0.000415
	9% difference	79% difference

5.3. CHAPTER SUMMARY

A unified modeling methodology for development of a single FEM to predict the physical response of an electronic package under thermal cycling, power cycling, and vibration loading was introduced. The unified modeling methodology is comprised of an enriched material model to accommodate time-, temperature-, and direction-dependent behavior of various materials in the assembly, and at the same time, has a geometry model that can accommodate thermal- and power-cycling induced low-cycle fatigue damage mechanism as well as vibration-induced high-cycle fatigue damage mechanism. The development of the unified FEM is complete. However, it now needs to be validated against experimental data before it can be used to develop predictive solder joint fatigue equations. Chapter 6 will validate the model for ATC and PC environments and then the low cycle ATC and PC predictive fatigue equations are developed in Chapter 7. Chapter

8 will validate the unified FEM for vibration loading and develop the high cycle predictive fatigue life equation for vibration loading.

CHAPTER 6

VALIDATION OF UNIFIED FEM MODEL FOR THERMAL CYCLING AND POWER CYCLING ENVIRONMENTS

6.1. INTRODUCTION

Before developing fatigue life prediction equations from the unified FEM, it is important to verify that the FEM is capturing the correct physical response of the CCGA and CBGA under ATC and PC environments. The following metrics from experiments are compared against the same metrics predicted by the FEM for each environment; deformation from laser moire interferometry is used for the ATC environment, and temperature from power cycling experiments is used for the PC environment. After the deformation predicted by the FEM has been validated through laser moire experiments, then predictive fatigue life equations can be developed against experimental ATC results with greater confidence. This chapter focuses on validating the deformation contours predicted by the unified FEM for CCGA and CBGA against laser moire deformation. Chapter 7 will develop the predictive fatigue life equations for CCGA and CBGA and ATC and PC environments and compare against experimental data.

6.2. LASER MOIRE INTERFEROMETRY

Previous laser moire interferometry work by Han et. al. on CCGA's and CBGA's was covered in the Background section. The intent of this current work is not to repeat Han's work, rather the intent is to use the deformations from laser moire interferometry to validate the finite element models developed in a later section. This will be done by comparing the deformation patterns between the laser moire experiments and the deformation predicted by the finite element models. If the FEM can be validated to predict the correct displacements for the laser moire strip specimen, which has a free surface on the cut section, then there is greater confidence that the predicted

displacements from the FEM for the full package are correct [123]. The following sections will show the results of the laser moire interferometry for CCGA and CBGA.

6.2.1. Equipment, Sample Preparation, and Procedure

A PEMI II portable moire system from Experimental Solid Mechanics was used to perform the experiments. The system includes a four beam interferometer along with a thermal oven for real-time measurements of deformations. The thermal oven is mechanically decoupled from the moire system so that vibrations from the thermal oven's fan will not affect the fringes. However, the sample holder is rigidly connected to the moire system through glass rods that allow no rigid body displacements to occur between the moire setup and sample. The thermal oven has liquid nitrogen cooling capability to reach temperatures as low as -55^{o}C. A schematic of the PEMI II is shown in Figure 6-1.

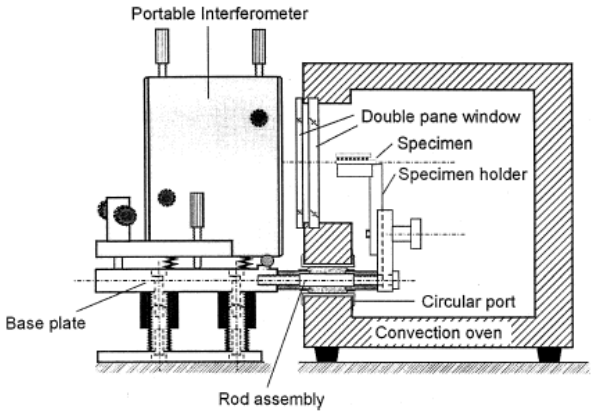


Figure 6-1. Schematic of the PEMI II moire setup for observing real-time deformations during thermal cycling. [108]

The sample is prepared by cross-sectioning to contain four rows of solder joints with one side polished flat to contain half a row of solder joints as shown in Figure 6-2. Cutting and polishing the tough, brittle ceramic substrate without damaging the soft solder is very difficult. The objective in preparing a sample for moire is to get the surface flat, not necessarily polished. A diamond saw was used to cut a strip with a width of four and half solder joints. The half row of solder joints was then polished on 15 micron diamond

sanding disc followed by a 6 micron diamond sanding disc until the surface was flat. It is very challenging not to round out the edges of the solder joints.

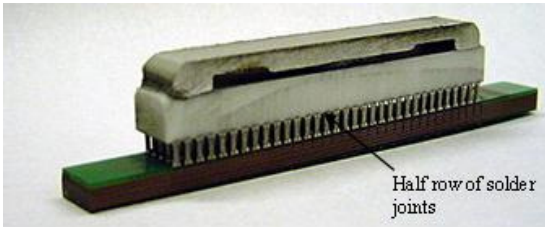


Figure 6-2. Cross-section of prepared sample before grating application

Once the sample is flat, the grating can then be attached to the sample, according to the following steps: A two part epoxy (Tra-Con F114® or equivalent such as Tra-Con F110®) is mixed being careful to minimize bubbles. Apply a small drop of epoxy to the grating surface. Spread the epoxy over an appropriate area using an optical lens tissue by dragging the tissue through the dab of epoxy. Spread as thin a layer as possible. Excess epoxy will cause bridging between the solder joints. Take the sample and gently apply to the grating. Be careful to minimize sliding and replacement of the sample. Push firmly once in place. A weight can be placed on top of the sample, but is not necessary. Let the epoxy cure completely. Once the sample is cured, remove the sample by applying a quick moment or shear force to the sample. The amount of force will depend on the amount of surface area that is attached to the grating. Be careful not too deform the sample when removing it from the grating. Take a new razor blade or X-acto knife and gently clean the edges if necessary. Be very careful as this can cause deformation of the grating at the edges. The thickness of the epoxy is generally 25µm and adds a negligible amount of stiffness to the system [104].

6.2.2. Laser Moire Studies on CCGA Package Assembly

The sample CCGA consisted of a 42.5 x 42.5 x 4mm CCGA with a 1.4mm thick conventional lid assembled onto a 2.8 mm PWB with 1089 balls on a 1.27 mm pitch. The CCGA was cross-sectioned to contain 4 rows of solder joints and one side was

ground flat using a 15 micron diamond sanding disc. The grating was then attached to the 'flat' side of the CCGA sample using an epoxy (Tra-Con F110®) which was cured for several days at room temperature. The first step of the moire procedure is to 'null' the deformation fringes so that ideally no deformation fringes appear at the temperature the grating was applied, i.e. the stress-free temperature. This 'nulling' at the stress-free temperature (25°C) is done by adjusting the reference grating until the number of fringes is near zero. The sample with the grating was then subjected to temperatures excursions of 60°C, 100°C, and then to 0°C as shown in Figure 6-3. The ramping rate was approximately 4°C/min. and once the oven reaches the designated temperature, the sample was dwelled at that temperature for ten minutes so that the sample reaches equilibrium temperature and there are no thermal gradients in the sample. A thermocouple attached to the specimen holder shown in Figure 6-2 was used to monitor the temperature and ensure the equilibrium temperature had been reached.

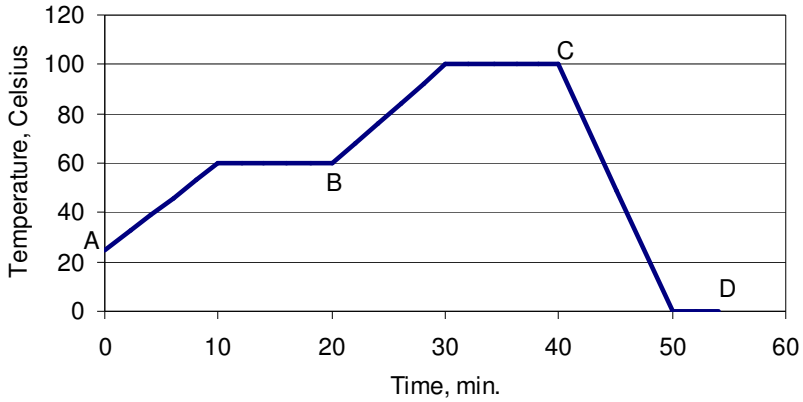


Figure 6-3. Temperature profile for laser moire interferometry of CCGA.

The resulting whole-field horizontal U and vertical V displacement fields were captured as shown in Figure 6-4. Only half the sample is shown as there is symmetry about the midline of the package.

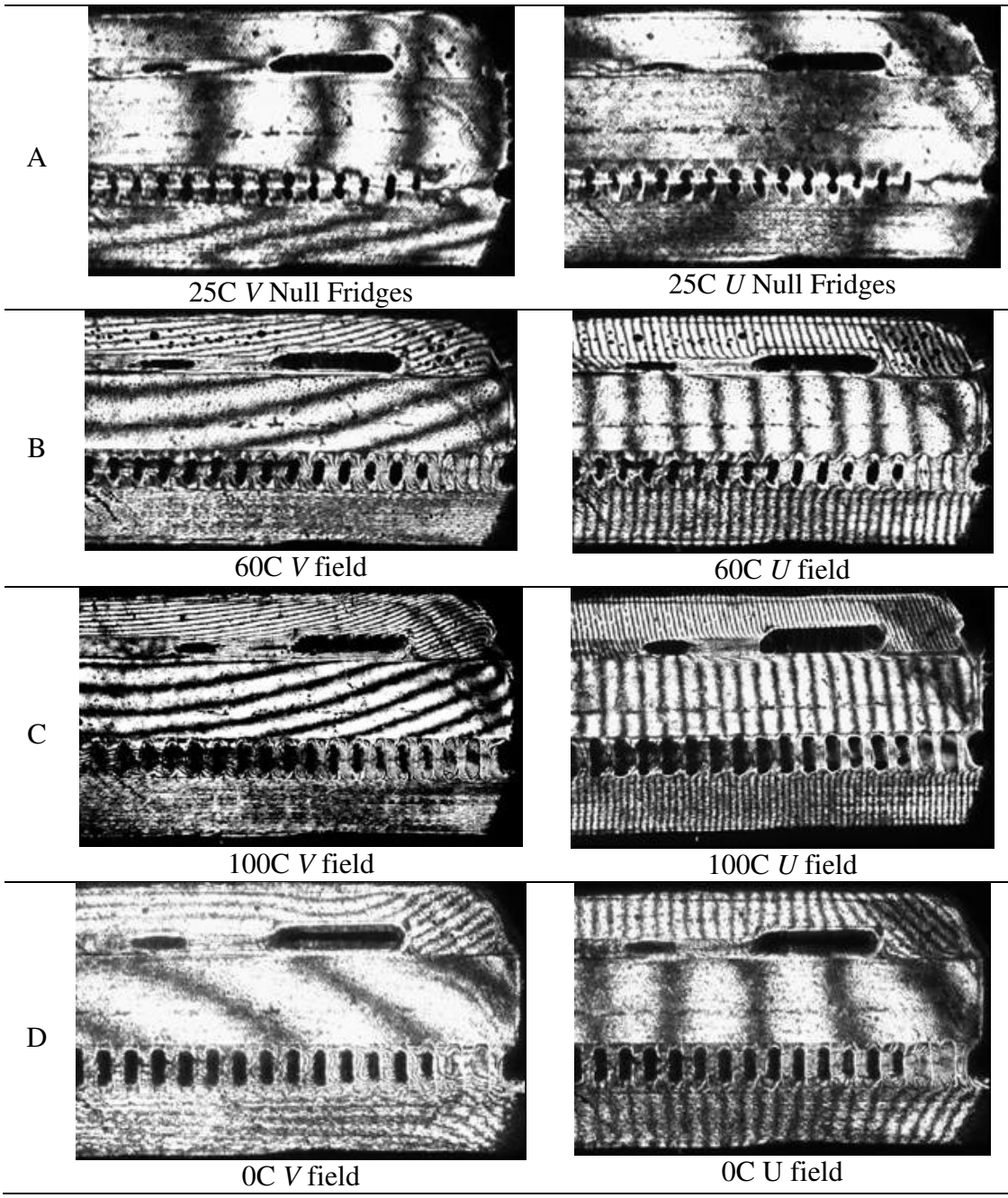


Figure 6-4.Whole-field displacement V field (left) and U field (right). Only the left half of the sample is shown.

As seen in the *V* and *U* displacement fields shown in Figure 6-4, the number of displacement fringes increases as the temperature increases. This is expected because the temperature difference ΔT relative to the stress-free temperature of 25°C continues to increase in a positive direction as the temperature increases and so the CTE driven displacement increases for both the ceramic substrate and FR4 board. At 0°C the

temperature difference ΔT relative to the stress-free temperature of 25°C is negative and the displacement and bending of the ceramic substrate and board is negative. The CTE of the board (18ppm/°C) is greater than the CTE of the ceramic substrate (6.8ppm/°C). As the temperature rises above 25°C the board expands more than the ceramic, and therefore the relative movement increases with temperature and bends the ceramic up. Likewise, below 25°C the board contracts more than the ceramic and causes a negative curvature. The difference in the displacement between the ceramic substrate and board, along with the coupling provided by the solder joints, causes the package to bend. The bending of the ceramic substrate can be seen by observing the slight $\delta V/\delta x$ gradient in the ceramic substrate. The displacements and bending are studied in greater detail in the following paragraphs.

The relative vertical displacement (bending) of the interposing ceramic substrate can be calculated using the V displacement fields shown in Figure 6-4. A plot of the ceramic substrate bending is shown in Figure 6-5. The displacements are relative to the middle of the package. The displacements are calculated along a line at the bottom of the substrate.

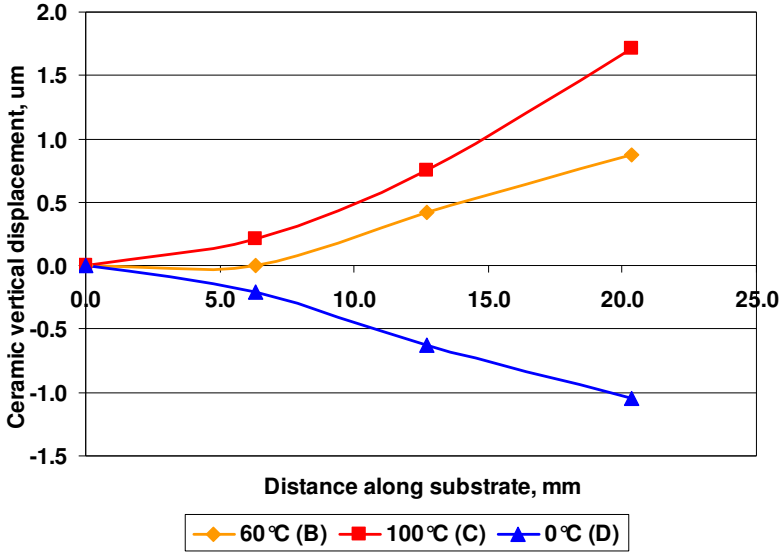


Figure 6-5. Vertical displacement of the ceramic substrate for CCGA

The bending of the ceramic substrate shows some nonlinearity as seen by the curvature. The amount of bending is minimal as seen by the maximum vertical displacement of ~1.75um. This is due to the high standoff height of the CCGA solder columns which can

accommodate large amounts of shear displacement. It will be seen later that the CBGA solder ball structure cannot accommodate such large shear displacements and causes the ceramic substrate to bend significantly. Figure 6-5 also shows that the curvature (and the warpage) is more at 100°C, compared to the curvature (and the warpage) at 60°C. Also, it is seen tha the interposing ceramic substrate warps upwards during heating of 60°C and 100°C, and warps down during cooling at 0°C. This warping is due to the fact that the lower CTE ceramic is on top and the higher CTE PWB is on bottom.

The relative horizontal *U* displacement between the substrate and board across the height of the solder joints is shown in Figure 6-6. The unrestrained relative displacement is also plotted in Figure 6-6 as a comparison. The unrestrained relative displacement is when the solder joints offer no resistance to free thermal expansion of the ceramic and board.

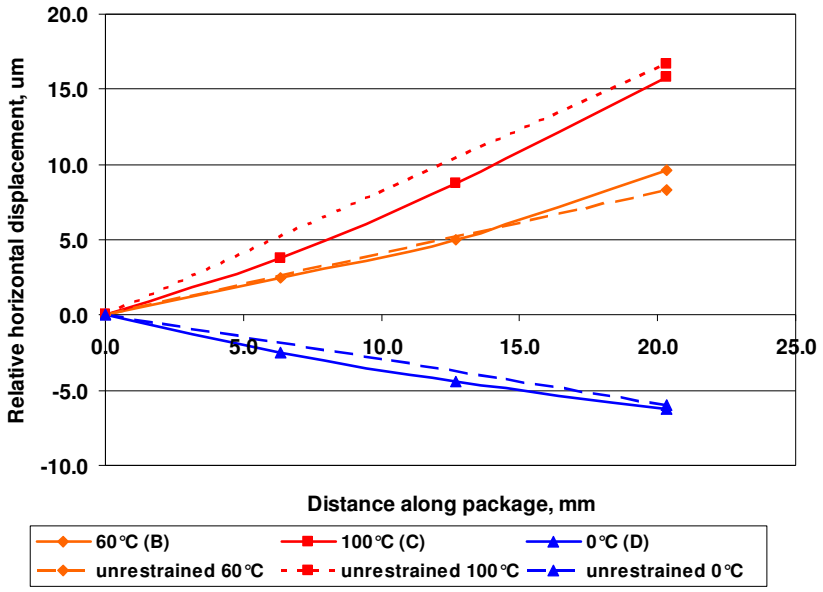


Figure 6-6. Relative horizontal displacement between ceramic substrate and board across the height of the solder joints for CCGA.

If the above measured relative displacements were compared to the unrestrained relative expansion of the board with respect to the ceramic ((α_{PWB}-α_{SUB}) x ΔT x DNP), it is seen that the measured displacements are nearly 95% of the unrestrained relative expansion. This indicates that the solder columns offer minimal resistance to the horizontal

expansion of the board and substrate. Han found a similar result for a CCGA with no lid attached [107].

A high resolution camera allows the displacement fields of the outermost solder joint to be captured as shown in Figure 6-7. The solder column is highlighted with a white border for clarity.

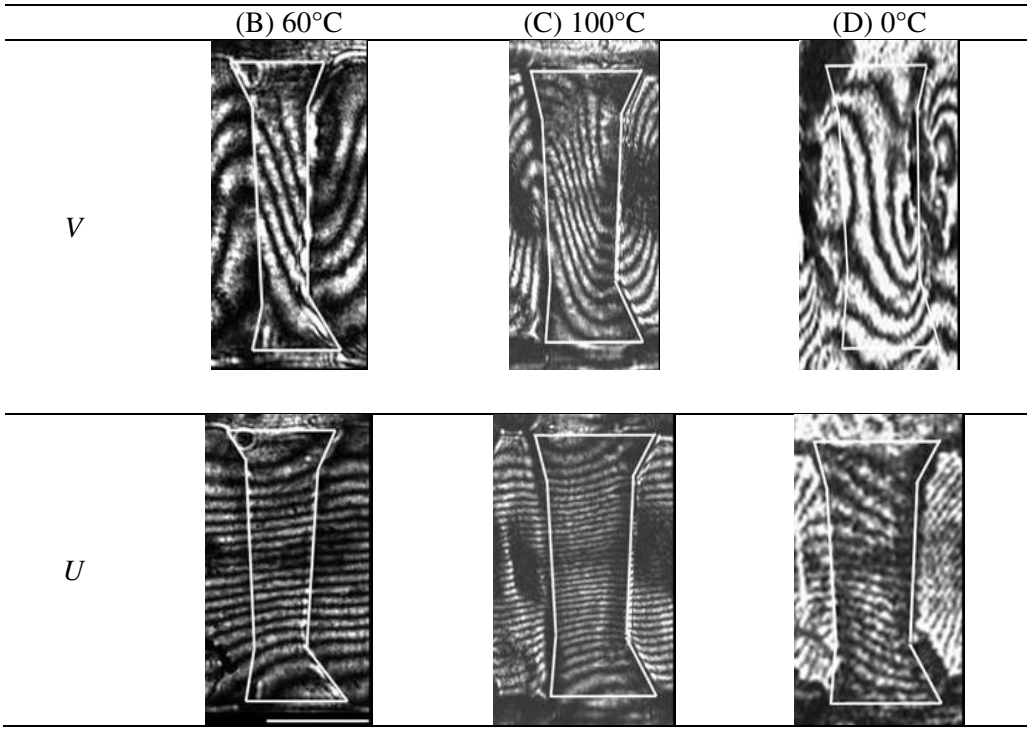
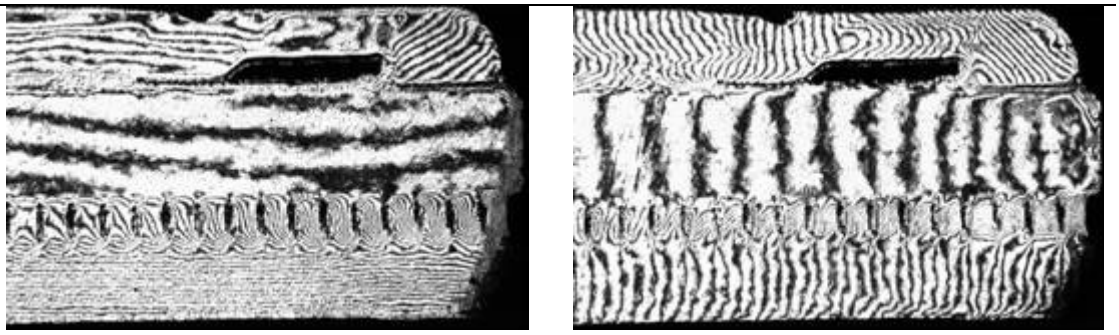


Figure 6-7. *U* and *V* displacement fields of the outermost CCGA solder joint

Shear displacement is large in the 90Pb10Sn solder as seen from the severe $\delta U/\delta y$ gradient in Figure 6-7. The horizontal orientation and close spacing of the *U* displacement shows the 90Pb10Sn solder column accommodates the CTE mismatch between the ceramic substrate and board by undergoing larger shear deformation in the 90Pb10Sn column. The stiffening effect of the 63Sn37Pb fillets can be seen by observing the deformation of the 90Pb10Sn solder column that is embedded in the 63Sn37 fillet has a smaller deformation gradient than the middle of 90Pb10Sn solder column.

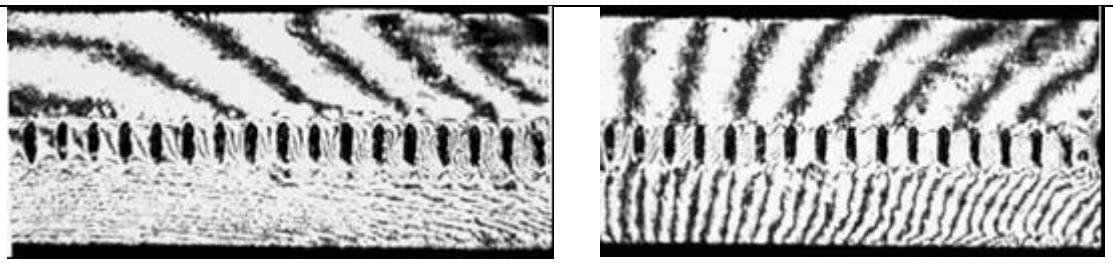
6.2.2.1. Effect of the aluminum lid on CCGA package assembly deformation

The effect of the lid in this study is to minimize the amount of bending that would otherwise occur. The aluminum lid CTE and stiffness are slightly greater than that of the board. Upon heating (cooling), the board applies a positive (negative) bending moment on the ceramic substrate. The aluminum lid provides an opposite and opposing bending moment on the ceramic substrate on the ceramic substrate. The net effect is to limit the amount of bending that would otherwise occur in the package. The aluminum lid does not completely negate the moment applied by the board because of three factors: 1) minimal contact area of the lid with the substrate; 2) a thin epoxy layer attaches the aluminum lid to the substrate; and 3) the stiffness of the aluminum lid is minimized as it is only 1.3mm thick. The effect of the lid can be seen in Figure 6-9 by comparing the *U* and *V* displacement fields at -20°C of a CCGA with and without the lid. A temperature below 0°C is chosen so the effect of the lid can be clearly seen by avoiding the relaxation in bending on the package assembly that can occur at higher temperatures due to solder creep relaxation reducing the coupling between the board and ceramic substrate.



-20°C *V* field -20°C *U* field

Figure 6-8. Effect of lid shown to minimize bending.



-20°C *V* field -20°C *U* field

Figure 6-9. CCGA with no lid shows package bending.

Figure 6-8 shows that at -20°C the bending in the CCGA package with the lid is nearly zero. This can be seen by observing that the *V* displacement field in the ceramic substrate and board are completely vertical, in other words there is no $\delta V/\delta x$ gradient. Similarly, the *U* displacement field in the ceramic substrate and board show uniform horizontal expansion characterized by the gradient $\delta U/\delta y$ being equal to zero. In Figure 6-9 which shows the CCGA with no lid, it can be seen the gradients $\delta V/\delta x$ and $\delta U/\delta y$ do exist indicating that there is bending in the package.

6.2.3. Laser Moire Studies on CBGA Package Assembly

The sample CBGA consisted of a lidless 15x15x0.738mm underfilled flip chip assembled onto a 25x25x1.8 mm alumina ceramic substrate with 552 balls on a 1.0 mm pitch. The CBGA was cross-sectioned to contain 4 rows of solder balls and one side was ground flat using a 15 micron diamond sanding disc. The grating was then attached to the 'flat' side of the CBGA sample using an epoxy (Tra-Con F114®) which was cured for several days at room temperature. Any residual deformation from the procedure to cross-section and apply the grating is minimal, and can be removed or accounted for as part of the moire setup. The sample was then subjected to the temperature profile shown in Figure 6-10 which goes down to -55°C, ramps successively to 125°C, and then ramps back down to room temperature 25°C.

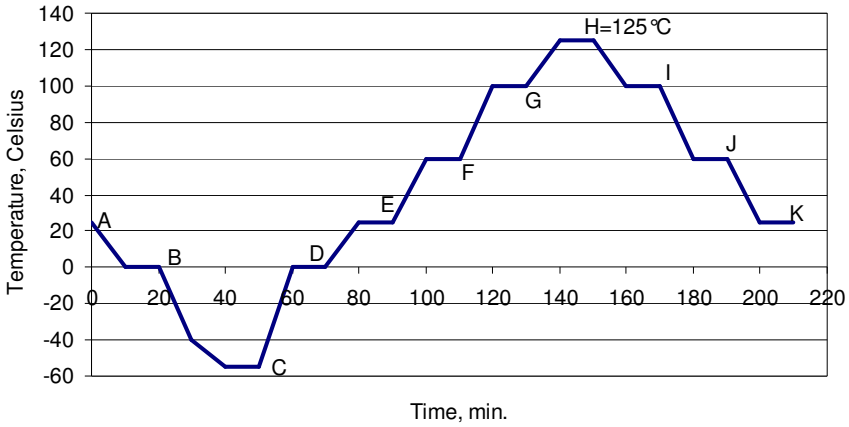
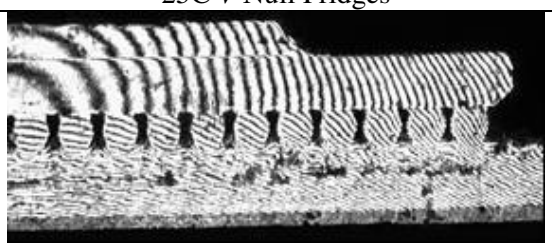
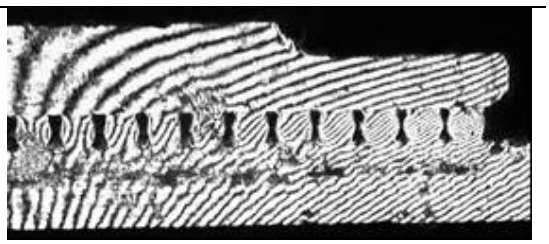


Figure 6-10. Temperature profile for laser moire interferometry of CBGA.

The temperature profile chosen for the CBGA laser moire interferometry study in Figure 6-3 mimicks an acclerated thermal cycling (ATC) profile. Dwells of ten minutes were included at points B, D, E, F, G, I, and J so that images could be captured to observe the deformation during these points. The images were captured at the end of the ten minute dwells to ensure an equilibrium temperature had been reached before capturing the image.

The resulting whole-field horizontal *U* and vertical *V* displacement fields were captured as shown in Figure 6-4. Only half the sample is shown as there is symmetry about the middle of the package.

A	 25C *V* Null Fridges	 25C *U* Null Fridges
C	 -55C *V* field	 -55C *U* field

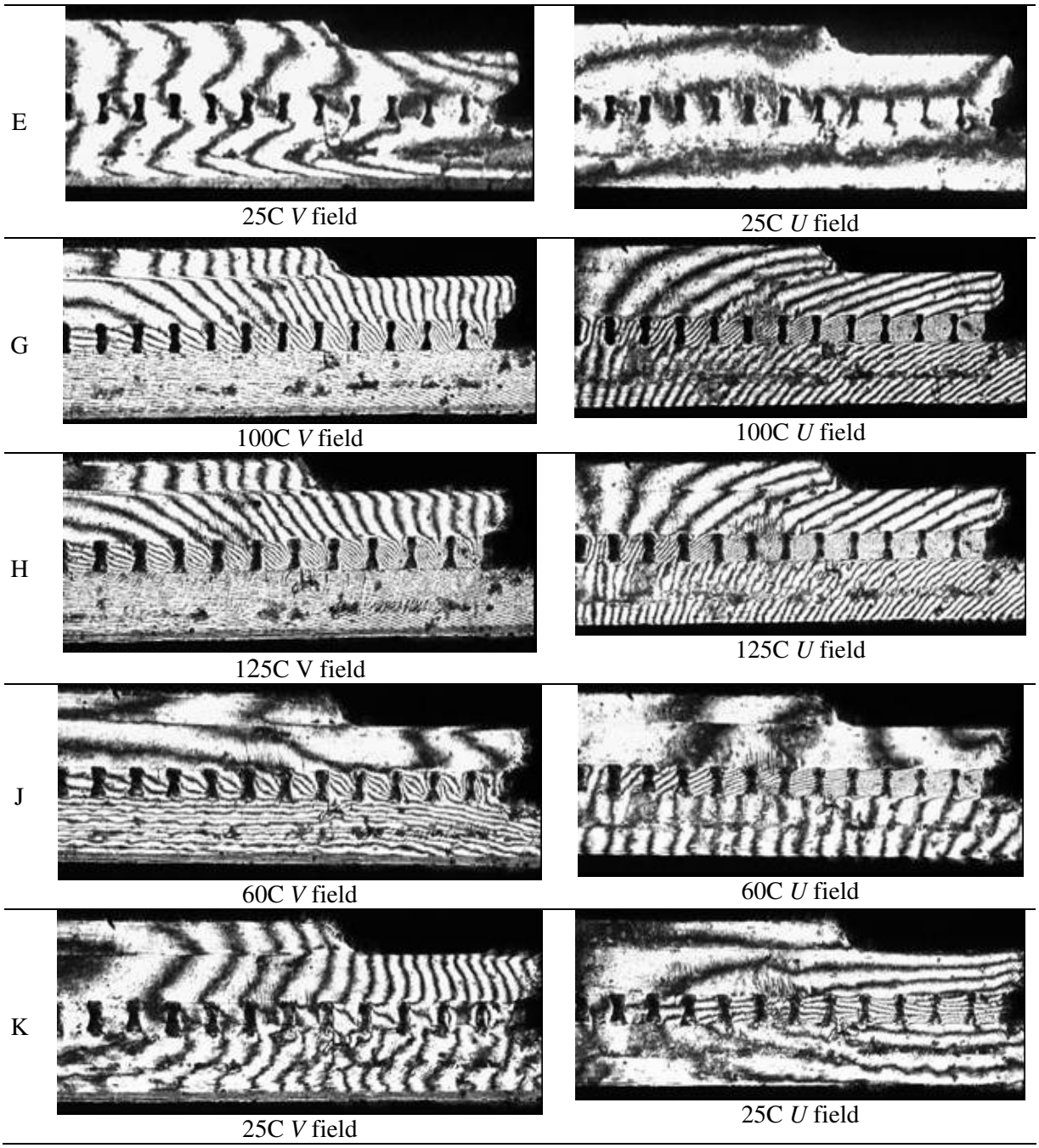


Figure 6-11. Whole-field displacement moire fringes for CBGA

An indication of severe package bending can be observed by noticing the vertical orientation of the *V* displacement fringes in Figure 6-11. This bending is due to the solder balls tightly coupling the CTE mismatch between the ceramic substrate and FR4

board. Figure 6-12 shows the amount of bending that occurs in the substrate at the outermost solder joint (number 12).

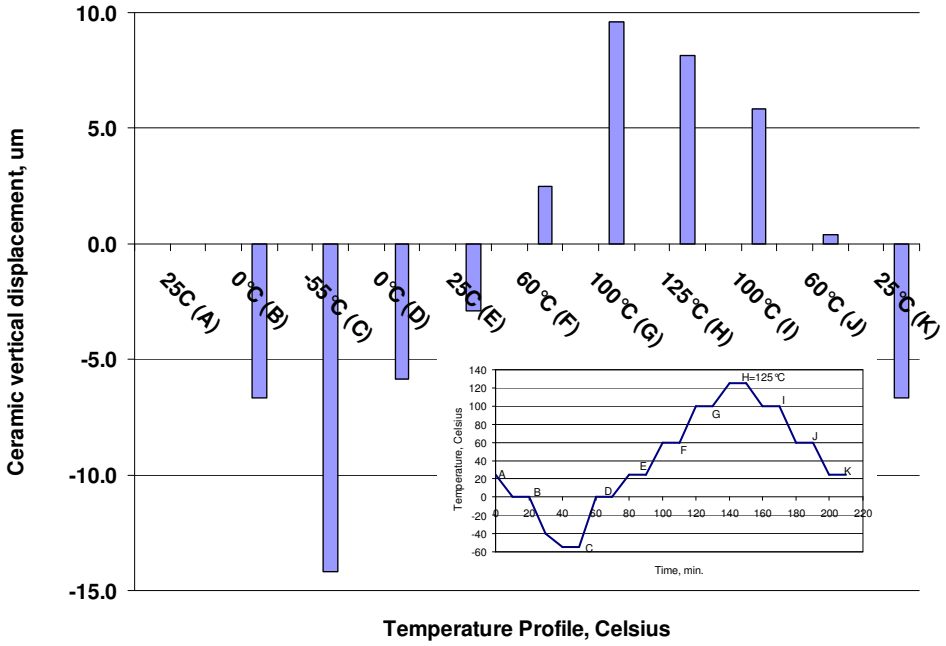


Figure 6-12. Ceramic substrate vertical displacement at outermost solder joint number 12 for CBGA

Figure 6-12 can be interpreted by the following:

- As the package cools from 25°C (A) to -55°C (C) there is significant negative bending of the ceramic substrate due to the CTE mismatch between the ceramic substrate (7ppm/°C) and the FR4 board (18ppm/°C). The maximum negative displacement is -14.2um.
- As the temperature rises from -55°C (C) back to room temperature 25°C (E) the ceramic substrate and FR4 board begin to expand back to their original dimensions. However, there is plastic deformation in the solder joints that causes a residual bending of -2.9um. If the deformation in the solder joints was completely elastic than three would be no residual deformation at 25°C (E).
- As the temperature rises from 25°C (E) to 100°C (G) the board expands more than the ceramic substrate and there is positive bending. In the solder joints there is continued

plastic deformation and an increasing amount of creep strain that causes stress relaxation. As the stress relaxes there is less plastic deformation that occurs. The maximum positive bending of 9.6um occurs at 100°C (G).

- As the temperature rises from 100°C (G) to 125°C (H) the rate of creep strain overcomes the rate of plastic strain and there is relaxation of the bending. The solder joints are allowing for greater shear deformation so that bending is not as severe. The bending drops form 9.6um at 100°C (G) to 8.1um at 125°C (H) due to creep strain causing stress relaxation in the solder balls.
- As the package cools from 125°C (H) to 60°C (J) the bending decreases as the ceramic substrate and FR4 board begin to contract. The amount of creep stress relaxation that has occurred makes 60°C effectively the new stress-free reference temperature. The 0.4um bending at the ramp down 60°C (J) is a significantly less than the 2.5um bending that occurred during the ramp up temperature of 60°C (F).
- As the package cools from 65°C (J) to 25°C (K) there is a negative displacement of -6.7um due to the continued contraction of the ceramic substrate and FR4 board. If the deformation in the solder joints was completely elastic than three would be no residual deformation at 25°C (E).

The lower standoff height of the solder balls do not allow for free thermal expansion for the ceramic substrate and board like the solder columns of the CCGA as shown in Figure 6-6. Figure 6-13 shows the relative horizontal movement between the ceramic substrate and board for the CBGA along with the relative free thermal expansion.

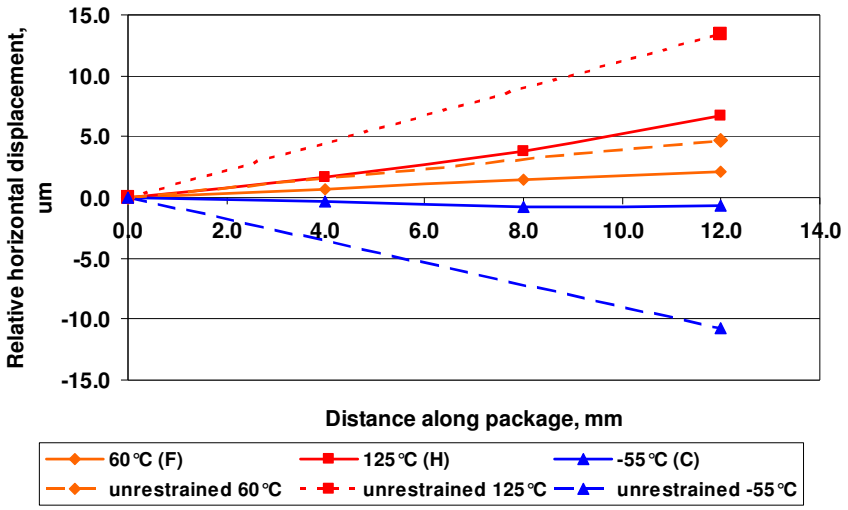
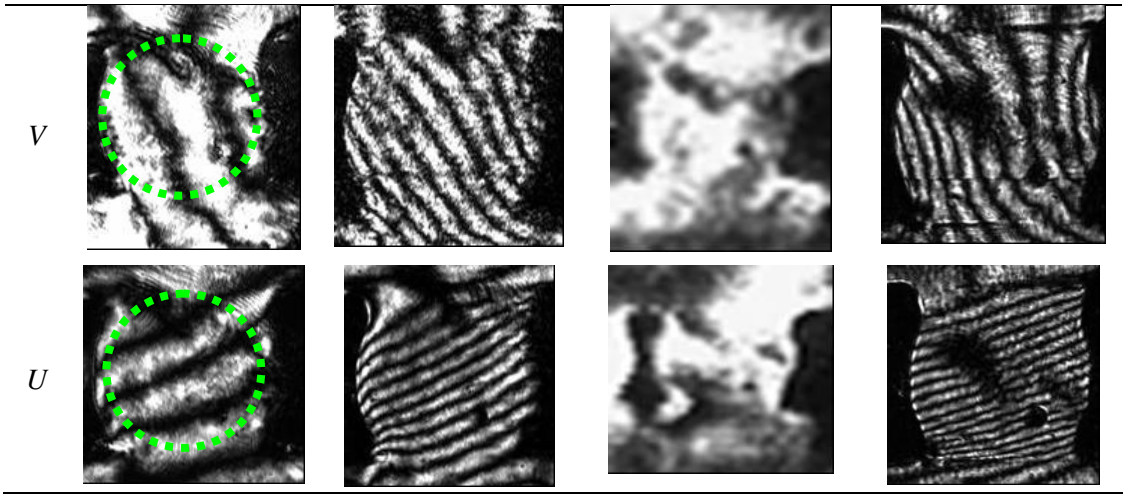


Figure 6-13. Relative horizontal displacement between ceramic substrate and board across the height of the solder joints for CBGA.

It is observed from Figure 6-13 that the horizontal free relative thermal expansion of the substrate and board is constrained by a factor of 2x or more due to the low standoff height of the solder balls. This restraining of the free thermal expansions causes the bending of the package described previously.

A high resolution camera allows the moire fringes outermost solder joint to captured in great detail as shown in Figure 6-14. The first set of *U* and *V* displacement fringes at 0°C (B) have the 90Pb10Sn solder ball outlined as a visual aid.



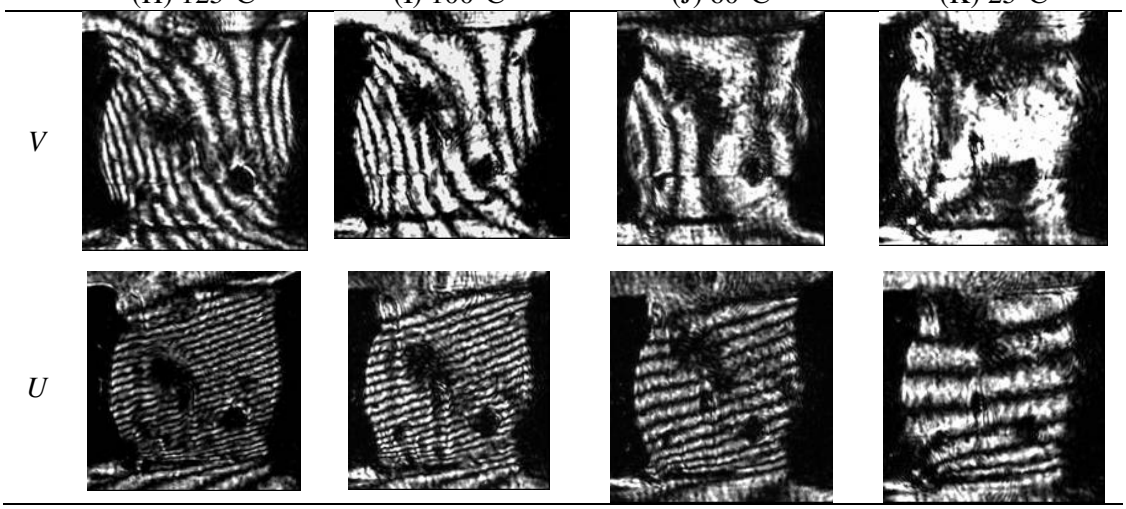


Figure 6-14 *U* and *V* displacement fields of the outermost CBGA solder joint

It can be seen that large strain gradients develop in the 63Sn37Pb fillets at the upper right substrate fillet and the lower left board fillet as shown in Figure 6-15 which is the *U* displacement field at -55°C. The two indicated sites are likely to be crack initiation points.

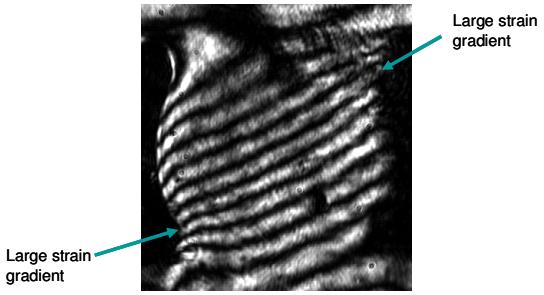


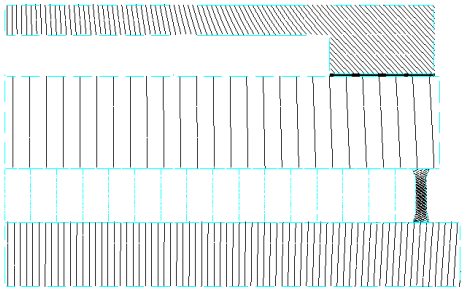
Figure 6-15. *U* displacement fringes at -55°C showing high strain gradients in 63Sn37Pb fillet

As the temperature increases up to 100°C (G) it can be seen that the strain gradients in the two indicated regions continue to increase as seen in Figure 6-14. When the temperature cools back down to 25°C (K) there are inelastic strains remaining. The highest inelastic strain gradients can be seen on the board side.

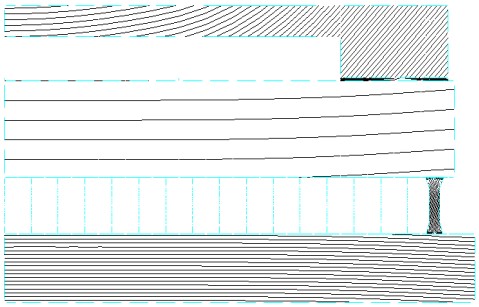
6.3. ACCELERATED THERMAL CYCLING VERIFICATION WITH LASER MOIRE INTERFEROMETRY

Laser moire interferometry from section 6.2 is used to validate the deformation predicted by the FEM under ATC for CCGA and CBGA. For the sake of brevity, only the results deformation contours at 100°C for CCGA and -55°C for CBGA will be compared.

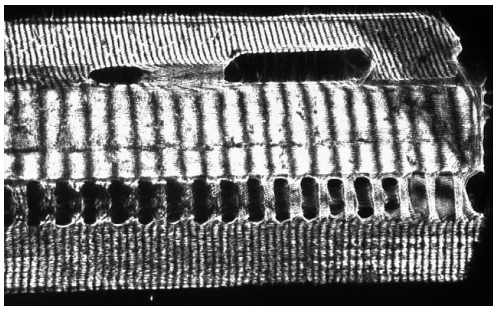
Figure 6-16 compares the horizontal U and vertical V displacement fields at 100°C from the laser moiré experiments and the FEM for the entire package assembly. Figure 6-17 shows the local U and V and displacement fields from laser moiré and FEM for the outermost solder joint at 100°C. It is seen from the Figure 6-16 and Figure 6-17 that the displacement contours agree well both in terms of numbers as well as orientation. The FEM is able to capture the relative displacements across the outermost DNP solder joint within 15%.



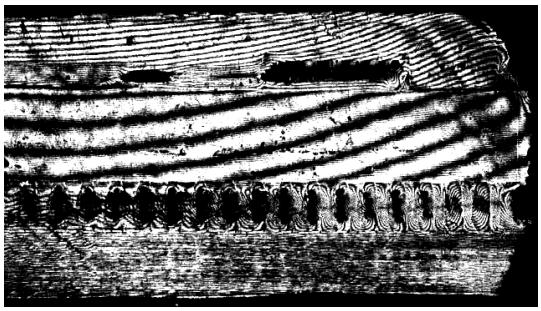
a) FEM *U* field



b) FEM *V* field

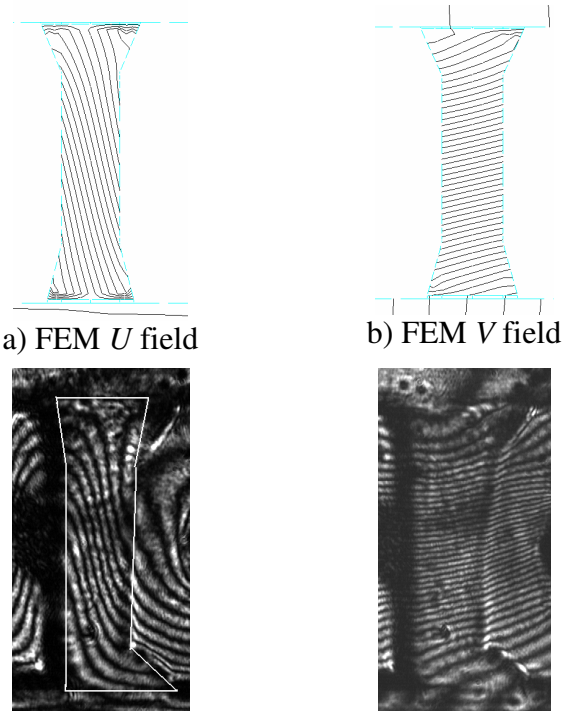


c) Laser Moire *U* field



d) Laser Moire *V* field

Figure 6-16. *U* and *V* whole-field displacement of FEM (a,b) and Laser Moire (c,d) at 100°C for CCGA

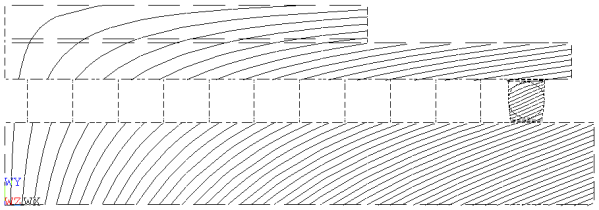


a) FEM *U* field b) FEM *V* field

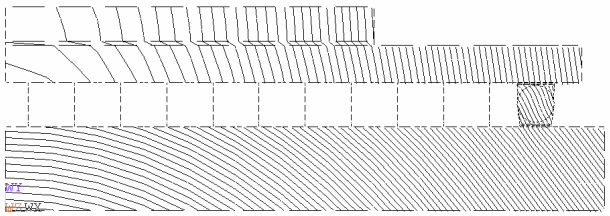
c) Laser Moire *U* field d) Laser Moire *V* field

Figure 6-17. *U* and *V* displacements of outermost solder joint at 100°C for FEM (a,b) and Laser Moire (c,d). for CCGA

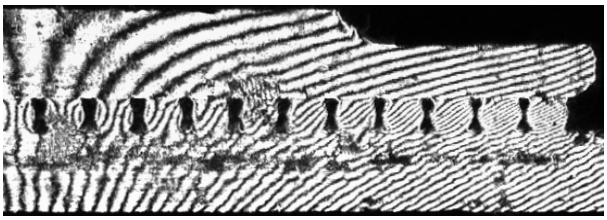
Figure 6-18 compares the horizontal *U* and vertical *V* displacement fields at -55°C from the laser moiré experiments and the FEM for the entire CBGA package assembly. Figure 6-19 shows the local U and V and displacement fields from laser moiré and FEM for the outermost solder joint at -55°C. It is seen from Figure 6-18 and Figure 6-19 that the displacement contours agree well both in terms of numbers as well as orientation and the FEM is able to capture the relative displacements across the outermost DNP solder ball within 15%.



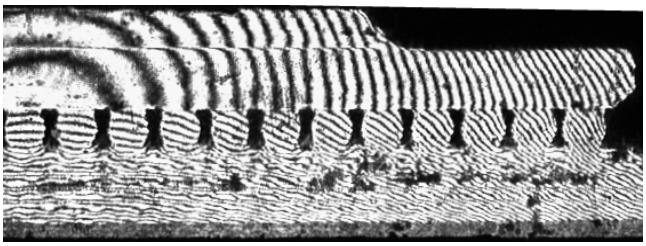
a) FEM *U* field



b) FEM *V* field

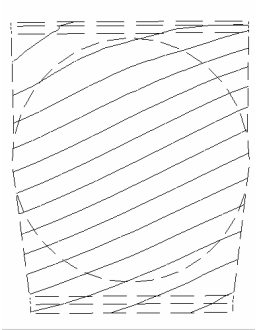


c) Laser Moire *U* field

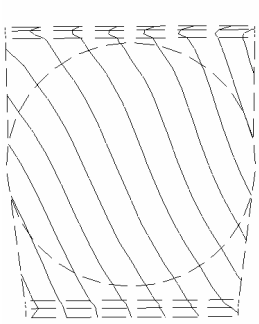


d) Laser Moire *V* field

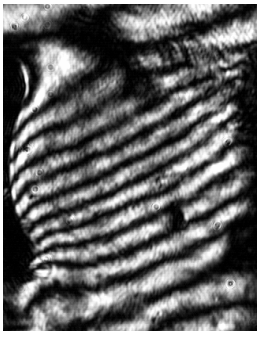
Figure 6-18. *U* and *V* whole-field displacement of FEM (a,b) and Laser Moire (c,d) at -55°C for CBGA



a) FEM *U* field



b) FEM *V* field



c) Laser Moire *U* field

d) Laser Moire *V* field

Figure 6-19. *U* and *V* displacements of outermost solder joint at -55°C for FEM (a,b) and Laser Moire (c,d). for CBGA

6.4. IMPORTANCE OF INCLUDING CREEP IN EVERY SOLDER JOINT OF FEM

Modeling the relaxation effects due to creep is important to capturing the warpage behavior of an electronic package. In order to validate the materials and FEM in this work, two FEM of the sample were created using the equivalent beam approach, one FEM included creep in the beams, and the second FEM only included creep in the outermost DNP detailed solder joint. Simulation of the real time laser moiré interferometry experiments from Cho and Han [108], presented in section 4.4.2, examined the relaxation of a CBGA component under a temperature cycle. The moiré and the FEM creep results show significant relaxation at temperatures above 75^0C, while the FEM with no creep in the equivalent beams overestimates the warpage at 100^0C by a factor greater than 2. The FEM that lack creep in the equivalent beams under predicts the inelastic work density by 25% which can have a significant effect on the predicted fatigue life.

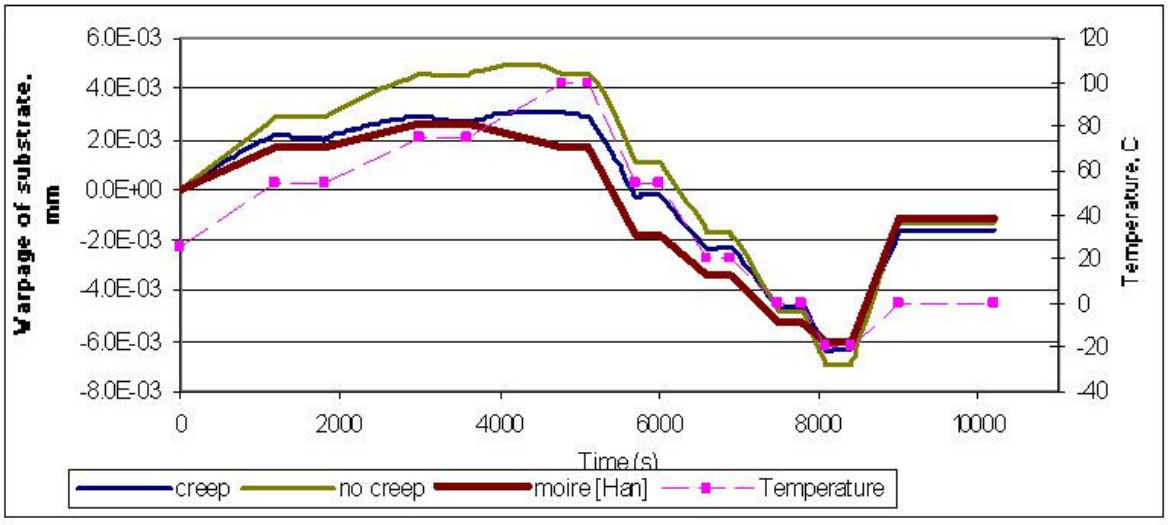


Figure 6-20. Effect of Modeling Creep in Equivalent Beams

6.5. POWER CYCLING PC VERIFICATION

6.5.1. Validation of PC Thermal Contours for CCGA

The power cycling thermal FEM for CCGA is validated against experiments performed by Martin, et. al [49]. Martin et. al [49] used a 40mm square, 2.3mm thick white alumina test vehicle with 29x29 array of columns on a 1.27mm pitch. An active 14.7mm square die with 15310 flip chip I/O connections was encapsulated with a 31 mm square aluminum lid that was 2mm thick. The package was mounted on a 124 mm x 114 mm FR4 6S8P test card. The package was assembled on cards of two thicknesses: 1.5mm thick with 14g (0.5 oz) copper layers, and 3.6mm card with 28g (1.0 oz) layers. The CTE values of the two cards were measured at 18.6 ppm/C for the 1.5mm card and 17.0 ppm/C for the 3.6mm card. The test vehicles were placed vertically on a drum with an airflow of 7m/s. The die was powered at 40 Watts and 35 Watts to achieve a temperature profile at the die center of 25/125^{0}C and 25/95^{0}C at 2 cph. Temperature values were measured at various points in the packages as shown in Table 6-1 so as to show the thermal gradient present in the package.

The experimental setup was simulated using the unified FEM by creating a CCGA with the same dimensions and applying appropriate convection coefficients to get a thermal profile that matched Table 6-1 when the die was powered at 40 Watts. The thermal conductivity of the board was estimated using a rule of mixtures for the in-plane and out-of-plane directions and resulted in 57.8 W/mK and 3.90 W/mK respectively. Figure 6-21 shows the thermal profile for the test vehicle on a 1.5mm thick PWB. On average, the predicted FEM temperatures are within 4% of experimental temperatures as shown in Table 6-1. Thus, the thermal behavior of the PC FEM is validated.

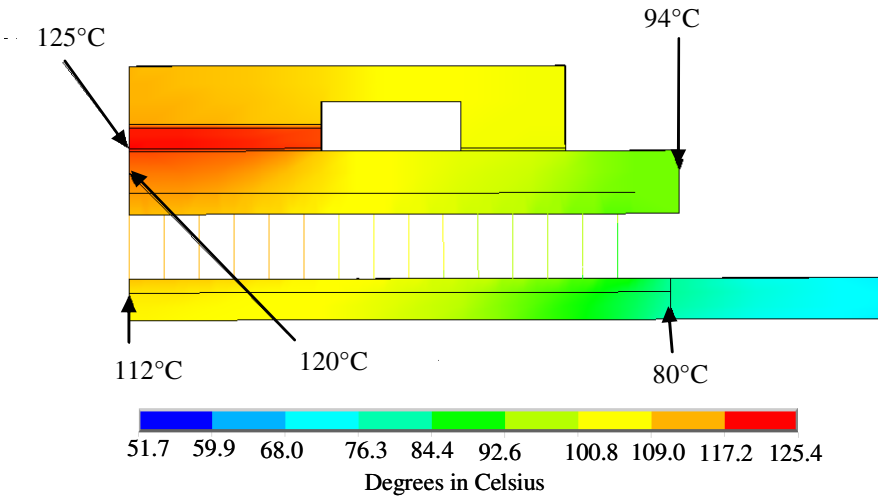


Figure 6-21. Temperature distribution of FEM used to valid PC FEM

Table 6-1. Comparison of experimental to FEM predicted temperatures.

Location	Experimental Temperature (^{o}C)	FEM Temperature (^{o}C)	Percent Difference (%)
Chip Center	127	125	2
Substrate Center	125	120	4
Substrate Corner	90	94	4
Card Center	113	112	1
Card Corner	72	80	11
			4% Average Percent Difference

6.5.2. Validation of PC Thermal Contours for CBGA

The power cycling thermal FEM for CBGA is validated against experimental data published by Yuan [124]. Yuan's CBGA package consisted of a lidless 13x13x0.625 mm flip chip with 1936 underfilled solder bumps assembled on a 32.5x32.5x3 mm ceramic substrate (Al2O3) with 625 solder balls. The CBGA package is attached to a 1S2P 107x156x1.8 mm FR4 board. Air flow with a velocity of 0.5 m/s to 4m/s was forced over the package in a wind tunnel. The die had a power of 5W uniformly distributed over its active surface. Yuan reported air-ambient thermal resistance for the different air flow velocities. The results from the FEM are compared with Yuan's results in Table 5. As seen, the FEM showed less than 8% error from the experiments.

Table 6-2. Validation of power cycling FEM for CBGA

	θ_{ja} (°C /W)	
Air Flow (m/s)	FEM	Yuan Experiment[124]
0.5	9.1	9.6
1	8.1	8.8
2	7.2	7.8

6.6. CHAPTER SUMMARY

The unified FEM for CBGA and CCGA was validated for ATC and PC environments by comparing displacements and temperatures with laser moire interferometry and power cycling data respectively. The next task in the unified modeling methodology is to develop low cycle predictive fatigue life equations for CCGA and CBGA under ATC and PC loading. Chapter 7 will develop a low cycle predictive fatigue life equations for 63Sn37Pb and 90Pb10Sn solders.

CHAPTER 7

DEVELOPMENT OF FATIGUE-LIFE PREDICTION EQUATIONS FOR EUTECTIC AND HIGH-LEAD SOLDER ALLOYS UNDER LOW CYCLE THERMAL AND POWER CYCLING

7.1. INTRODUCTION

In chapter 6, the deformation contours of CCGA and CBGA predicted by FEM under isothermal excursions and the temperature gradients predicted by FEM under power cycling were validated against experimental data. In this chapter, fatigue life equations for lead-tin solder under ATC and PC environments will be developed and validated using various sets of experimental data.

A Coffin-Manson type equation as in Eq. (4.7) or Eq. (4.10) is used to determine the solder joint fatigue life. Typically, ATC and PC are considered low cycle fatigue failures ($<10^4$ cycles) and inelastic or total strain is typically used as a damage parameter. While for the vibration environment, the fatigue life is in the high cycle regime ($>10^5$ cycles) and stress amplitude or elastic strain range is used as a damage parameter [78]. There has been some contention as to whether high cycle vibration fatigue in solders is strictly elastic in nature and that plasticity needs to be included in high cycle vibration fatigue [71, 96]. However, for the purposes of this work, it is assumed that high cycle fatigue is elastic in nature. In this work, inelastic strain range per cycle $\Delta\varepsilon_{in}$ and the Vonmises stress amplitude per cycle σ^{i}_{vm} are used as damage parameters for the ATC/PC and vibration environments respectively.

7.2. CBGA: 63SN37PB SOLDER JOINT FATIGE LIFE

CBGA's fail primarily in the 63Sn37Pb solder paste fillets and not in the 90PB10Sn solder ball, as observed previously in section 6.2.3. Thus a fatigue model for 63Sn37Pb solder under low cycle ATC and PC conditions will be developed in this section.

Seven experimental ATC tests as shown in Table 7-1 from literature are used for the development of Coffin-Manson type equations. As seen in Table 7-1, experimental tests cover a range of substrate size, substrate thickness, board thickness, solder pitch, substrate material, and thermal cycling conditions.

Table 7-1. CBGA experimental data from literature used to develop predictive equation for ATC and PC

Case [reference]	Substrate Size (mm)	Substrate Thickness (mm)	Board Thickness (mm)	Pitch	Substrate Material	ATC	Die Attached?	$N50_{exp}$
1 [125]	25x25	0.8	1.57	1.27	HICTE Glass	-55/110 2cph	NO	2160
2 [126]	25x25	1.65	1.57	1.00	Al_2O_3	0/100 2cph	YES	1870
3 [112, 127]	32.5x32.5	2.9	1.83	1.27	Al_2O_3	0/100 3cph	NO	1100
4 [128]	32.5x32.5	0.8	1.83	1.27	Al_2O_3	-55/110 2cph	NO	990
5 [126]	25x25	1.65	1.57	1.00	Al_2O_3	-55/110 2cph	YES	540
6 [128]	32.5x32.5	1.8	1.83	1.27	Al_2O_3	-55/110 2cph	NO	470
7 [128]	32.5x32.5	2.9	1.83	1.27	Al_2O_3	-55/110 2cph	NO	320

These experimental cases are modeled through the unified 3D FEM developed in chapter 5 which use equivalent beams to represent the solder balls with appropriate time- , temperature-, and direction-dependent properties for the materials in the assembly. Using thermal cycling simulations, damage parameters such as inelastic strain range $\Delta\varepsilon_{in}$, total strain range $\Delta\varepsilon_{tot}$, strain energy density ΔW_{tot}, etc. are obtained from the finite-element models. The calculation of these damage paramters was described previously in chapter 4.

The damage parameter obtained from the finite-element models for each one of the cases is plotted against $N50_{exp}$ data, and using such plots, two fatigue equations are examined to predict CBGA solder joint fatigue life; a typical Coffin-Manson model as in Eq. (4.7), and a crack growth equation shown in Eq (7.1).

$$N_{50} = \frac{a}{da/dN} = \frac{a}{K_3(\Psi)^{K_4}} \tag{7.1}$$

where: N_{50} is the number of cycles for 50% (or 63%) of the samples to fail, a is the length of the final length of the crack and equal to the substrate/board pad diameter in mm, da/dN is the rate of crack growth in mm/cycle, K_3 and K_4 are constants found through least squares regression, and Ψ is a damage parameter. Crack initiation is neglected as it only accounts for 10% of the total fatigue life for a ceramic package [129], and much of the literature data do not report crack lengths as a function of cycles.

Nonlinear regression is performed to determine the constants C_1 and n in Eq. (4.7) and the constants K_3 and K_4 in (7.1) for three damage parameters of inelastic strain range per cycle $\Delta\varepsilon_{in}$, total strain range per cycle, and total strain energy density per cycle. Simulations of the cases in Table 7-1with the appropriate ggeometries were run using the unified FEM developed in chapter 5. The damage parameters were calculated after stabilization of the hysterisis loop which took 3 thermal cycles. Regression analysis was used to relate the damage parameter and the experimental N_0 so that the constants C_1, n, for Eq.(4.7), and constants K_3,K_4 in Eq. (7.1) could be solved for. A value of 0.86mm which represents the substrate pad diameter was used for the crack length paramter a in Eq. (7.1). Two software programs, EXCEL[130] and JMP 5.1 [131] are used to determine the constants. For the development of a given model, all of the seven sets of experimental data in Table 7-1 were used. Table 7-2 lists the results along with the error sum of squares (SSE). Error sum of squares (SSE) is the sum of the square of residuals between the fitted model and the experimental data points, and the smallest value of SSE is one indicator of the "best-fit" model.

For the same damage parameter and predictive equation, the two software packages estimate different values of C_1, n, K_3, and K_4, and thus provide different values of SSE, as seen in Table 7-2. For example, Model 1 (EXCEL) estimates a constant n of -1.980 that matches the commonly used value of 2 in literature [30, 127, 132], whereas Model 2 (JMP) estimates a constant n of -1.720. However, as indicated by the SSE values, Model 1 (EXCEL) does not provide the 'best' fit as does Model 2 (JMP). Similarly, between Models 3 and 4 which use the same damage parameter $\Delta\varepsilon_{tot}$, Model 4 (JMP) provides a better fit compared to Model 3 (EXCEL), as indicated by the SSE values. JMP consistently provides a better fit indicated by the lower SSE values in Table 7-2 for the same damage parameter and predictive equation.

Table 7-2. Developed Coffin-Manson and crack growth equations

Equation	Model	Parameter	Software	C_1	n	SSE
$N_{50}=C_1(\Psi)^n$ Eq. (4.7)	1	$\Delta\varepsilon_{in}$	EXCEL	0.0255	-1.985	146016
	2		JMP	0.107	-1.720	99160
	3	$\Delta\varepsilon_{tot}$	EXCEL	0.0093	-2.280	94200
	4		JMP	0.0332	-2.034	56525
	5	ΔW_{tot}	EXCEL	15.79	-1.438	102388
	6		JMP	25.25	-1.280	53004
	Model	Parameter	Software	K_3	K_4	SSE
$N_{50}=\frac{a}{K_3(\Psi)^{K_4}}$ Eq. (7.1)	7	$\Delta\varepsilon_{in}$	EXCEL	36.46	2.003	204815
	8		JMP	7.13	1.700	131975
	9	$\Delta\varepsilon_{tot}$	EXCEL	102.8	2.300	103714
	10		JMP	24.3	2.030	68094
	11	ΔW_{tot}	EXCEL	0.056	1.453	102388
	12		JMP	0.033	1.286	54326

Several trends and relationships can be observed in Table 7-2 concerning the fitted constaints C_1, n, K_3, and K_4 . The first observation is that for all damage models involving a strain range $\Delta\varepsilon$ as a damage parameter, the exponents n and K_4 are close to the value of 2, such that $N_{50} \propto \Delta\varepsilon^{-2}$. Likewise, for all damage models involving the total strain energy density ΔW_{tot}, the exponents n and K_3 are close to a value of 1.3, such that $N_{50} \propto \Delta W_{tot}^{-1.3}$. From classical mechanics, the linear (elastic) strain energy density $W \propto \varepsilon^2$ where E is the Young's modulus, so it should not come as a surprise that when nonlinearity (inelasticity) is included that we see $N_{50} \propto \Delta\varepsilon^{-2}$ and $N_{50} \propto \Delta W_{tot}^{-1.3}$. The second observation is that the values of C_1 are proportional to $1/K_4$, as may be expected based on the forms of Eq. (4.7) and Eq. (7.1). These two observations indicate that the

two fatigue equations are similar in form, the three damage parameters are related, and any of the models in Table 7-2 may prove sufficient in predicting fatigue life.

Having made the above observations, a single fatigue equation must still be chosen as a basis for the predictive polynomial fatigue equation under ATC. Among the two fatigue life equations, Eq. (4.7) and Eq. (7.1), and among the three damage parameters ($\Delta\varepsilon_{in}$, $\Delta\varepsilon_{tot}$, and ΔW_{tot}), it appears that Model 12 is the preferred model because: (1) its SSE value is small; (2) it represents crack growth behavior and therefore, can account for different solder joint sizes; (3) it uses total strain energy density ΔW_{tot} as the damage metric which in general is a better damage metric than other two damage metrics as seen in Table 7-1 through the SSE values; and (4) it represents the monotonic inverse relationship between the damage metric and the fatigue life for each one of the test cases specified in Table 7-1. Equation (7.2) shows Model 12 which is the chosen model used for predicting solder joint fatigue failure in this chapter:

$$N_{50} = \frac{a}{0.033(\Delta W_{tot})^{1.286}} \tag{7.2}$$

where, a is the final crack length and equal to the substrate/board pad diameter, and ΔW_{tot} is the total strain energy density per cycle.

In some cases, it may be more convenient or proper to choose a model based on a strain damage parameter, rather than a strain energy density parameter. In that case, then model 4 as shown in Eq.(7.3) is chosen:

$$N_{50} = 0.033(\Delta\varepsilon_{tot})^{-2.04} \tag{7.3}$$

Table 7-3 uses two more cases from literature to validate the chosen fatigue equation. These cases were not used in the development of the fatigue equations and thus are useful for showing the validity of the model.

Table 7-3. CBGA experimental data from literature used to validate predictive equation for ATC

Case [ref.]	Substrate Size (mm)	Substrate Thickness (mm)	Board Thickness (mm)	Pitch	ATC	Die Attached?	N_{50exp}	N_{50} (Eq. (7.2)	N_{50} (Eq. (7.3)
8 [126]	25x25	1.65	1.57	1.00	0/100 2cph	YES (no lid)	2240	1950	2270
9 [126]	32x32	1	1.83	1.27	0/100 2cph	NO	2700	2280	2827

From Table 7-3 it can be seen that the predicted values are within 20% of the experimental values for either fatigue equation.

7.3. CCGA: 90PB10SN SOLDER JOINT FATIGE LIFE

The fatigue model developed for 63Sn37Pb solder in CBGAs will not work for CCGA's due to the failure being in the 90Pb10Sn solder column.

7.3.1. ATC CCGA Test

ATC test was performed in a Thermatron ATS-195V thermal shock chamber. The thermal cycle was -25/105^{o}C at 2cph, as measured by thermocouples on the test vehicles. Figure 7-1 shows the test box design to hold the test vehicles in as uniform a thermal environment as possible.

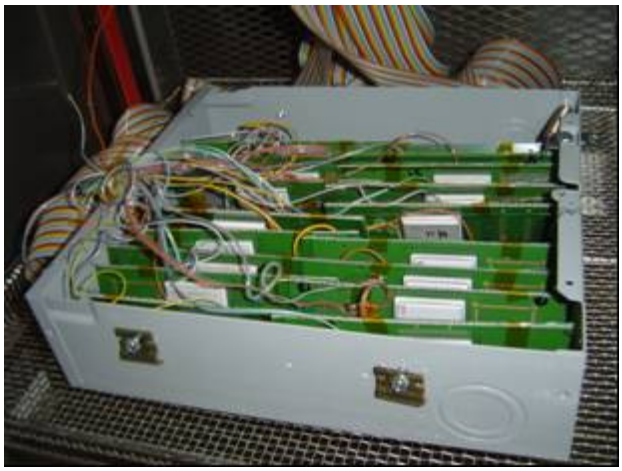


Figure 7-1. Test box for ATC tests.

The electrical resistances of daisy chain rings R_0, R_1, and R_{XX} was continuously monitored to determine when failure occurred. Failure was defined to occur when the

resistance of the ring exceeded 100 ohms for two consecutive cycles. The fatigue life cycle N_T under ATC alone was determined in this manner and are presented in Table 7-4.

Table 7-4. Results of CCGA ATC fatigue life tests.

	Fatigue Cycles		
Test Vehicle	R_0	R_1	R_{XX}
A	750	800	1835
B	1182	1438	1593
C	1228	1284	1587
D	1189	1220	1586
E	1226	1190	1768
F	1315	1409	1474
Mean	1148	1224	1640
Median	1207	1252	1590
Standard Deviation	200	230	134

From Table 7-4 it can be seen that the outermost solder joints of chain R_0 have the shortest mean fatigue life at 1148 cycles. As the DNP decreases the solder joints experience greater mean fatigue life indicated by daisy chain R_1 having a mean fatigue life of 1224 and the innermost joints of daisy chain R_{XX} having a mean fatigue life of 1640. A mean fatigue life of 1148 cycles from the outermost daisy chain R_0 will be used in conjuction with other experimental data from literature to develop the fatigue life equation for 90Pb10Sn solder as outlined in the following section.

7.3.2. Development of Fatigue Life Equation for 90Pb10Sn solder under ATC and PC Environments

In order to develop the constants C_1 and n for the Coffin-Manson fatigue equations for 90Pb10Sn solder, mostly literature data and the in-house tests at Georgia Tech are simulated in the unified FEM. Table 7-5 shows the critical design parameters and type of environment for the 10 cases chosen. Table 7-5 includes CCGAs with a variety of parameters including substrate size, substrate thickness, board thickness, pitch, presence of a lid, and presence of a die.

Table 7-5. CCGA experimental data from literature used to develop predictive equation for ATC and PC

Case [ref.]	Substrate Size (mm)	Substrate Thickness (mm)	Board Thickness (mm)	Pitch (mm)	Lid	Load	Die	$N50_{exp}$
1 [133]	42.5x42.5	3.0	1.57	1.27	-	-55/110 2cph	-	763
2 [133]	42.5x42.5	1.4	2.79	1.27	-	-55/110 2cph	-	895
3 [133]	42.5x42.5	1.4	1.57	1.27	-	-55/110 2cph	-	1035
4 [133]	42.5x42.5	3.0	2.79	1.27	Yes	-55/110 2cph	-	715
5 [133]	42.5x42.5	3.0	1.57	1.27	Yes	-55/110 2cph	-	636
6 [133]	42.5x42.5	1.4	1.57	1.27	Yes	-55/110 2cph	-	607
7 [in-house]	42.5x42.5	4.0	2.79	1.27	Yes	-25/105 2cph	-	1148
8 [49]	40.0x40.0	2.3	1.5	1.27	Yes	0/100 2cph	Y	1730
9 [49]	40.0x40.0	2.3	3.6	1.27	Yes	0/100 2cph	Y	2290
10 [49]	40.0x40.0	2.3	3.6	1.27	Yes	0/100 2cph PC	Y	11000

Each of the ten cases in Table 7-5 were simulated with the FEM and the total strain range per cycle is plotted against the experimental fatigue life as shown in Figure 7-2. A strain energy damage parameter was found to be effective for 63Sn37PB solders, however a strain range damage parameter was found to be more effective for 90Pb10Sn solder. In order for a strain energy damage parameter to be effective, the area of the stress-strain hysterisis loop must change considerably among the different cases presented in Table 7-5. The area of stress-strain hysterisis loop changes little for the 90Pb10Sn solder column for two reasons: 1) 90Pb10Sn has a higher creep resistance than 63Sn37Pb and thus the inelastic stress relaxation and change in area of the hysterisis loop is minimized; 2) the geometry of solder column results in lower stresses, particularly shear stresses, than in the solder ball case, thus minimizing the potential for change in area of the

hysterisis loop, among the different cases studied. Therefore, inelastic strain is considered a better damage metric for CCGA packages with 90Pb10Sn solder.

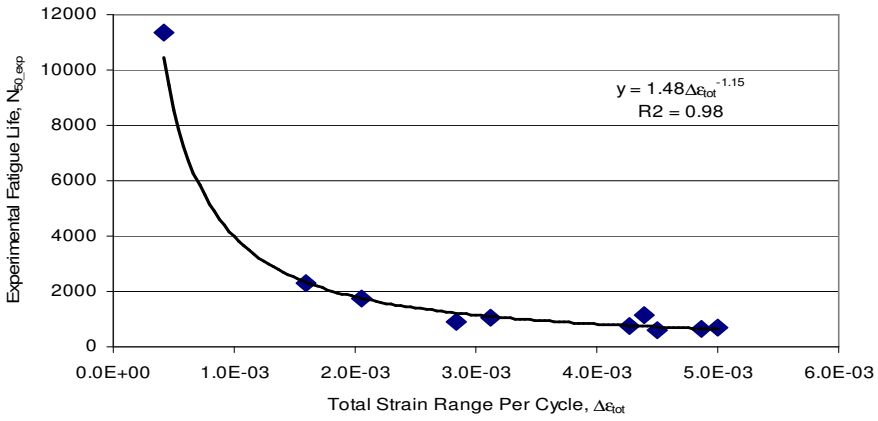


Figure 7-2. Total strain range strain vs fatigue life

The constants C_1 and n were found through least squares regression to be 1.48 and -1.15 respectively. The R^2 goodness of fit value of 0.98 is good and gives greater confidence that the FEM is able to effectively predict the solder joint fatigue life for a variety of design parameters under ATC and PC. Equation (7.4) shows the fatigue life model used for the ATC and PC environments.

$$N_{50}=1.48\ (\Delta\varepsilon_{tot})^{-1.15} \tag{7.4}$$

Four additional axperiments from literature data as shown in Table 7-6 were simulated in the unified FEM and the fatigue life calculated using Eq. (7.4). These cases were not used in the development of the fatigue equations and thus are useful for showing the validity of the model. From Table 7-6 it can be seen that the predicted values are within 10% of the experimental values.

Table 7-6. CCGA experimental data from literature used to validate predictive equation for ATC and PC.

Case [ref.]	Substrate Size (mm)	Substrate Thickness (mm)	Board Thk. (mm)	Pitch (mm)	Lid	Load	Die	$N50_{exp}$	$N50_{pred}$ (Eq. (7.4))
1 [133]	42.5x42.5	3.0	2.79	1.27	-	-55/110 2cph	-	775	803
2 [133]	42.5x42.5	1.4	2.79	1.27	Yes	-55/110 2cph	-	647	720
3 [134]	52.5x52.5	2.85	2.54	1.00	Direct Lid Attach	0/100 2cph	Y	2000	1975
4 [49]	40.0x40.0	2.3	1.5	1.27	Yes	0/100 2cph PC	Y	7940	7233

7.4. CHAPTER SUMMARY

Predictive fatigue life equations for CBGA and CCGA under low cycle ATC and PC were developed using both in-house experimental data and literature experimental data. Chapter 8 will now validate the unified FEM for vibration loading and develop the high cycle predictive fatigue life equation for CCGAs containing 90Pb10Sn solder.

CHAPTER 8

VALIDATION OF UNIFIED FEM AND DEVELOPMENT OF FATIGUE LIFE MODEL FOR VIBRATION

The unified FEM has been validated for ATC and PC in chapter 6. Predictive fatigue life equations for low cycle ATC and PC environments were developed in chapter 7. This chapter will focus on validating the unified FEM for vibration and developing a predictive fatigue life equation under a high cycle vibration environment.

This chapter will develop an experimental and a modeling approach that can accurately determine the solder joint behavior of electronic components under vibration conditions. In particular, this paper discusses the out-of-plane sinusoidal vibration experiments at 1G, numerical modeling, and fatigue life prediction for a 42.5mm x 42.5mm x 4mm 1089 I/O CCGA package on a 133mm x 56mm x 2.8mm FR4 board. Detailed investigation and characterization involving dye-and-pry analysis, microstructural examination, and numerical modeling enabled the development of a general high cycle stress-based equation for 90Pb10Sn solder that is applicable to any component under sinusoidal loading. The developed approach will be applied to a number of cases including a CCGA package with a heat sink as well as a CCGA package subjected to frequency sweeps. It is seen that the predictions from the developed model agree well with experimental data and that the developed model can map the evolution of solder damage across all solder joints and also, can provide important design recommendations in terms of solder joint location as well as heat sink attachment.

8.1. VIBRATION EXPERIMENTAL SETUP AND RESULTS

8.1.1. Vibration Experiment Setup

The experimental setup consisted of a Ling Dynamic Systems V722™ shaker with a DVC48 power amplifier. The test vehicles were 42.5mm x 42.5mm x 4mm CCGA

electronic packages with 1089 solder joints assembled onto 137mm long x 56mm wide x 2.8mm thick FR4 board as described in chapter 4. The test vehicles were then clamped between four 12.7 mm thick x 19.0 mm wide plates to create clamped-clamped boundary conditions as shown in Figure 8-1. Two accelerometers were used to characterize the system; one accelerometer was placed on the shaker fixture to measure the input acceleration to the system, G_{in}, and the second accelerometer was placed on top of the CCGA package to measure the output acceleration of the CCGA, G_{out}. As the mass of the accelerometer (7 g) was comparable to the mass of the CCGA (33 g), the mass of the accelerometer was included in the simulations to capture the natural frequency and vibration behavior of the CCGA assembly [63].

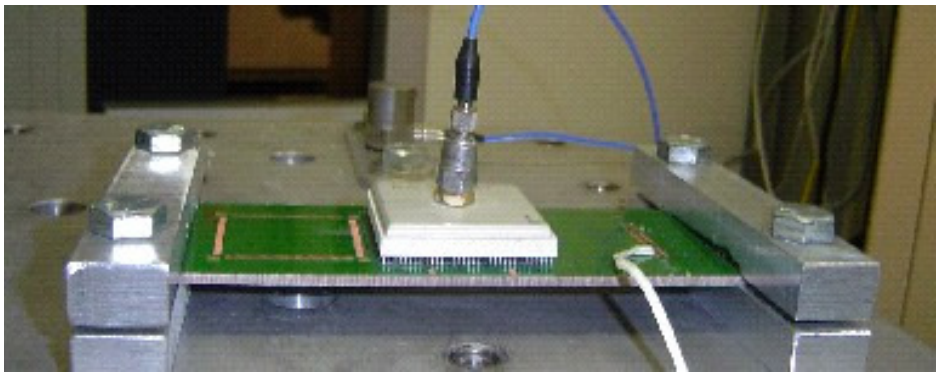


Figure 8-1. Experimental setup for CCGA on FR4 board with clamped edges.

In order to best learn the dynamic characteristics of the CCGA and understand how failure occurs, sinusoidal vibration tests are chosen rather than random vibration tests. This is because random vibration tests excite multiple natural frequencies at once and make it difficult to systematically study how and where damage is occurring.

8.1.2. Experimental Results

Linear sweep tests from 40-500Hz at 0.1G were performed on five test vehicles, labeled A thru E, to characterize the natural frequency f_n, and the damping ratio ξ,of the system. For example, Figure 8-2 shows the output acceleration G_{out} when test vehicle A was swept from 40-500 Hz with an input acceleration of 0.1G. For the sake of clarity, the

results from 270 Hz to 350 Hz are presented, as the output acceleration beyond this range is roughly constant at 0.1G.

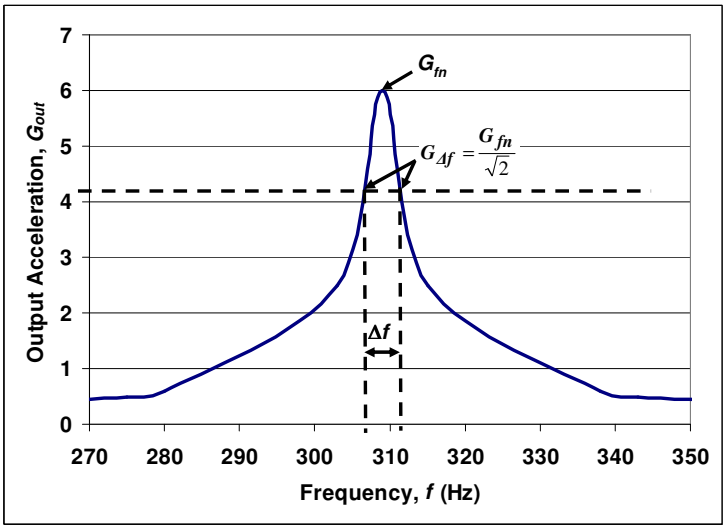


Figure 8-2. Linear sweep test for test vehicle A to determine the damping ratio ξ.

As seen in Figure 8-2, the peak output acceleration occurs near 308 Hz. This is the natural frequency of the assembly as determined by the vibration experiments, and this value agrees with the natural frequency determined through previous analytical modeling by the authors in [63]. From Figure 8-2, it is possible to determine the damping ratio of the system using equation (8.1) [110]

$$\xi = \frac{\Delta f}{2 f_n} \tag{8.1}$$

where Δf is the bandwidth of the half power points, $G_{\Delta f}$. and f_n is the natural frequency. The half power points, $G_{\Delta f}$, are defined as the two points defined according to equation (8.2) [110]

$$G_{\Delta f} = \frac{G_{fn}}{\sqrt{2}} \tag{8.2}$$

where G_{fn} is the output acceleration at the natural frequency.

Using G_{fn} = 6.0G, f_n =308 Hz and Δf = 5Hz, the damping ratio ξ was found to be approximately 0.008 which is indicative of a lightly damped system.

After characterization of the CCGA assembly, a fatigue failure test was conducted by subjecting the assembly to 1G input acceleration at f_n until failure of each daisy chain occurred sequentially, with the exception of test vehicle D which was used for subsequent dye and pry analysis after only daisy chain R_0 failed. Table 8-1 presents the results for the five test vehicles A, B, C, D, and E; as seen from Table 8-1, the mean f_n of the test vehicle is 308 Hz with a standard deviation of 14.2 Hz. This indicates that the CCGA package and FR4 board fabrication and assembly of CCGA package on FR4 board were nearly uniform. Also, the damping ratio of all of the test vehicles is between 0.008 and 0.009 indicating a high degree of uniformity in the test vehicle fabrication, experimental set-up, and experimental procedure. The f_n and G_{out} were repeatable within ±0.1 Hz and ±0.2G respectively for each test vehicle.

Table 8-1. Results for sinusoidal vibration testing of G_{in} =1G at f_n

	Characteristics			Cycles to Failure		
Test Vehicle	f_n, Natural Frequency (Hz)	G_{out}, Maximum Output Acceleration (G)	Damping ratio	Daisy chain R_0	Daisy chain R_1	Daisy chain R_{XX}
A	309	40.7	0.008	3.56E+05	1.03E+06	3.10E+06
B	285	58.0	0.009	1.20E+05	2.10E+05	6.07E+05
C	315	45.4	0.008	1.76E+05	4.16E+05	2.19E+06
D	305	38.4	0.008	7.92E+05	*	*
E	323	53.7	0.009	1.40E+05	2.77E+05	1.41E+06
Mean	308	47.3	0.0084	3.16E+05	4.82E+05	1.83E6
Standard Deviation	14.2	8.4	0.0005	2.81E+05	3.72E+05	1.06E6

*No experimental data, as the sample was used for dye and pry analysis after R0 failure

Table 8-1 presents the measured values of f_n, damping ratio ξ, G_{out}, and the number of cycles to failure for the three daisy chains under study. In general, it is seen that f_n and ξ for the test vehicles are roughly the same with a standard deviation that is less than 6% of the mean value.

The fatigue life of each daisy chain ring is dependent upon the output acceleration G_{out}, as seen in Figure 8-3 which plots the fatigue life of the output acceleration G_{out} against

the fatigue life for each daisy chain ring. It is also seen that the fatigue failure occurs first in the daisy chain R_0, then in the daisy chain R_1, and then in R_{xx}. This indicates that the outermost solder joints near the clamped edges undergo maximum damage, and then progressively less for the interior solder joints. Furthermore, it is seen that when G_{out} is high, fatigue life is low. As G_{out} is measured on the package, higher acceleration of the package is likely to induce greater damage in the solder joints. Variations in G_{out} and thus fatigue life values for different test vehicles can be attributed to potential variations in the clamping of the test vehicles and potential assembly process variations.

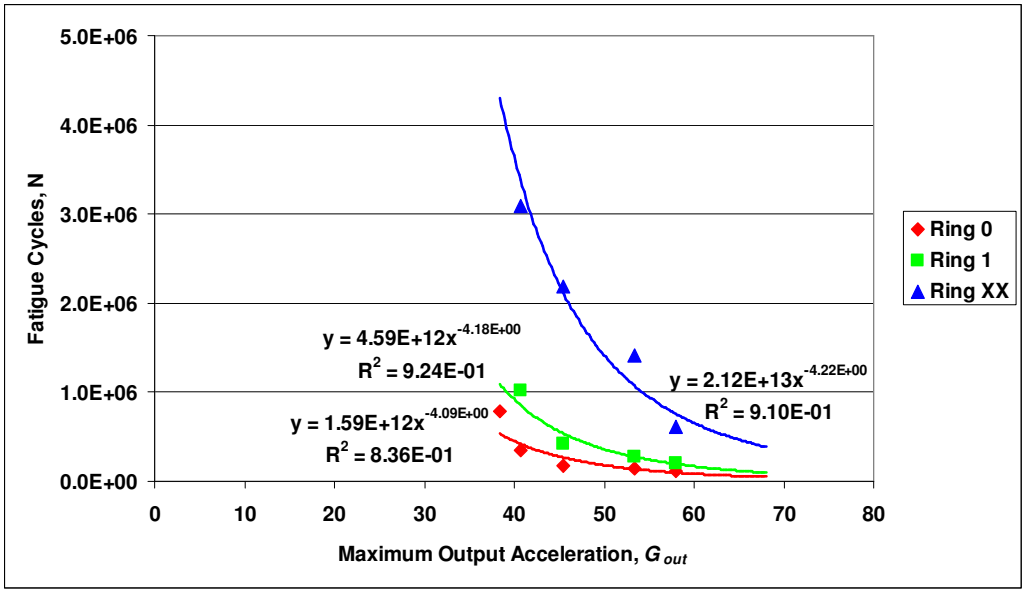


Figure 8-3. G_{out} versus fatigue life cycles for Ring 0, Ring 1, and Ring XX.

8.2. FEM MODAL ANALYSIS AND STRESS DISTRIBUTION.

Predicting the correct fundamental frequencies and corresponding mode shapes is critical in developing an accurate vibration fatigue life model. Figure 8-4 shows the results of a modal analysis on the FEM to find the first three fundamental frequencies and corresponding mode shapes of the experimental CCGA test vehicle. The contours represent vertical displacement and are for visual purpose. It should be pointed out that the scale is intentionally left out as each mode shape is normalized by its modal mass. The resulting mode shapes are typical of a fixed-fixed beam, however, the ceramic

substrate and solder columns cause local stiffening of the PWB under the CCGA. Only the first mode is used in this study where out-of-plane sinusoidal test at the natural frequency will be performed. However future studies involving random vibration over a spectrum of frequencies will require contributions of several fundamental mode shapes. Previous modeling work ECTC 2004 paper and another publication (ASME JEP) also show the validity of the FEM model with vibration data.

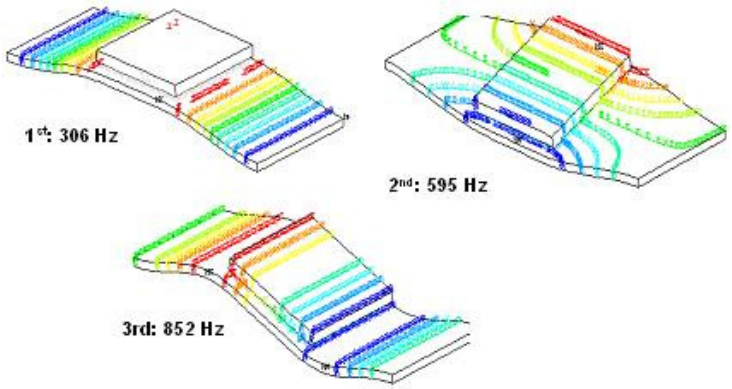


Figure 8-4. FEM mode shapes of 1089 CCGA Package on FR4 Board

It can be seen from Figure 8-4 that the mode shape and numerical value of the fundamental frequency at 306Hz closely matches the mode shape and fundamental frequency of 308Hz predicted by the analytical model as shown in Figure 4-22. The analytical model developed in chapter 4 and the FEM can be used to investigate higher natural frequencies and modes shapes as shown in Table 8-2. Knowledge of the higher order mode shapes will be useful for random vibrations analysis where all modes are excited simultaneously and other failure mechanisms can be identified.

Table 8-2. Fundamental Frequency of FR4 with 1089 I/O Component

	Fundamental Frequency (Hz)		
Mode	FEM	Analytical	Experiments
1	306	308	308
2	595	-	
3	852	885	

Figure 8-5 shows the absolute value of the axial equivalent beam stresses σ_{yy} distribution for each solder joint under a 1G harmonic acceleration at the natural frequency of the

system. A damping ratio ξ of 0.008 as determined from the vibration analysis was used in the harmonic analysis. As seen, high stresses occur in the solder joint array in the corners and at the outermost columns closest to the clamped boundary conditions. These predicted high stresses indicate that the corner joints are likely to fail first.

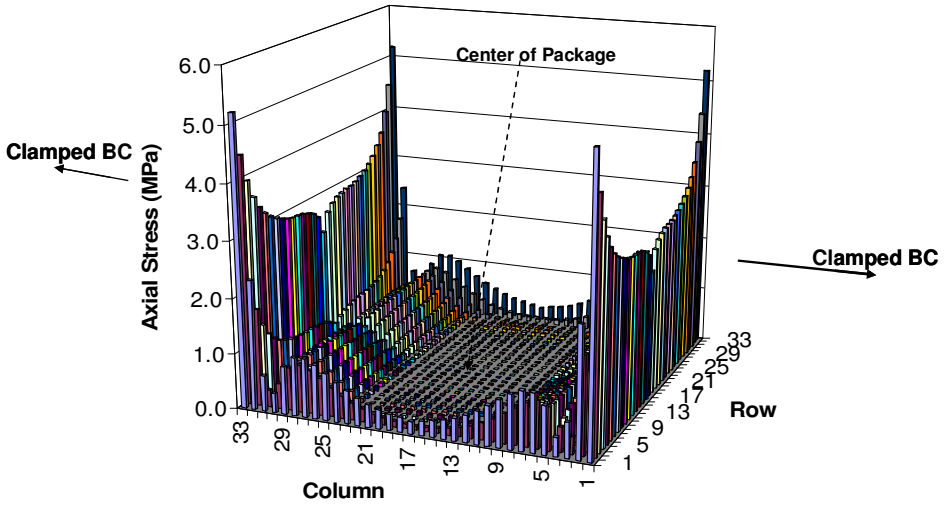


Figure 8-5. Axial stress distribution of CCGA solder columns under vibration

Further validation of the FEM for vibration loading is done by comparing the failed joints in a dye-n-pry analysis with the stress distribution in the solder joints shown in Figure 8-5.

8.3. DYE-AND-PRY ANALYSIS OF TEST VEHICLE D: SOLDER JOINT FAILURE LOCATION

As mentioned earlier, test vehicle D was first subjected to a linear sweep test to find f_n and ξ, and then was driven at a G_{in} of 1G at f_n until failure of daisy chain R_0 occurred. Test vehicle D was then subjected to dye-and-pry analysis.

The dye-and-pry analysis is a means to see the failure and crack distribution in solder joint after failure. Upon failure, the test vehicle was dried and blown clean with compressed air, immersed in red Dykem® steel layout fluid for ten minutes, and then baked at 70°C for 15 minutes. The ceramic substrate was then carefully removed from the FR4 board. A high force of approximately 400lbf. is required to remove the

substrate, and therefore, a special removal fixture was developed to limit the bending of the FR4 board and prevent breaking of the brittle ceramic substrate. The removal fixture consists of a U-shaped steel frame with five bolts at strategic points. The FR4 board is rigidly attached to a base plate with bolts to minimize bending during substrate removal. The U shaped steel frame fits around the underside periphery of the ceramic substrate to provide support while the five bolts are tightened. As the five bolts are tightened the ceramic substrate is slowly removed as shown in Figure 8-6.

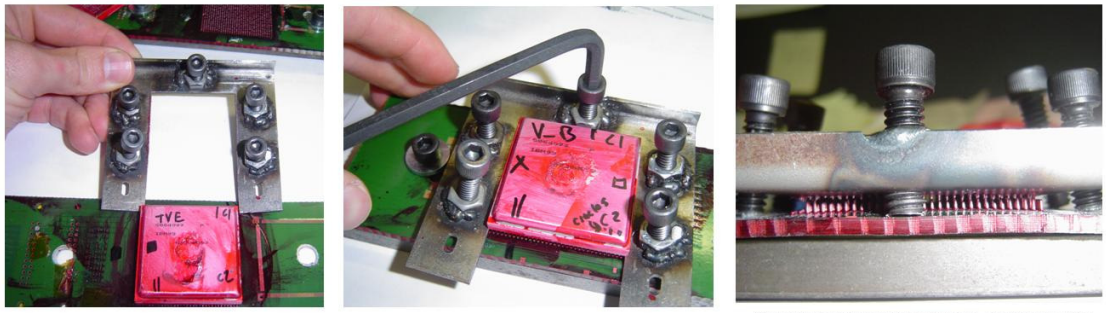


Figure 8-6. Special removal fixture to remove substrate from board for dye-n-pry analysis

Once the substrate is removed, the crack propagation in the solder joints can be determined by the amount of dye penetration. The portion of crack that grew during the vibration testing will be dyed red, while the remaining portion will be undyed. Figure 8-7 shows the failure and crack distribution from the dye and pry analysis.

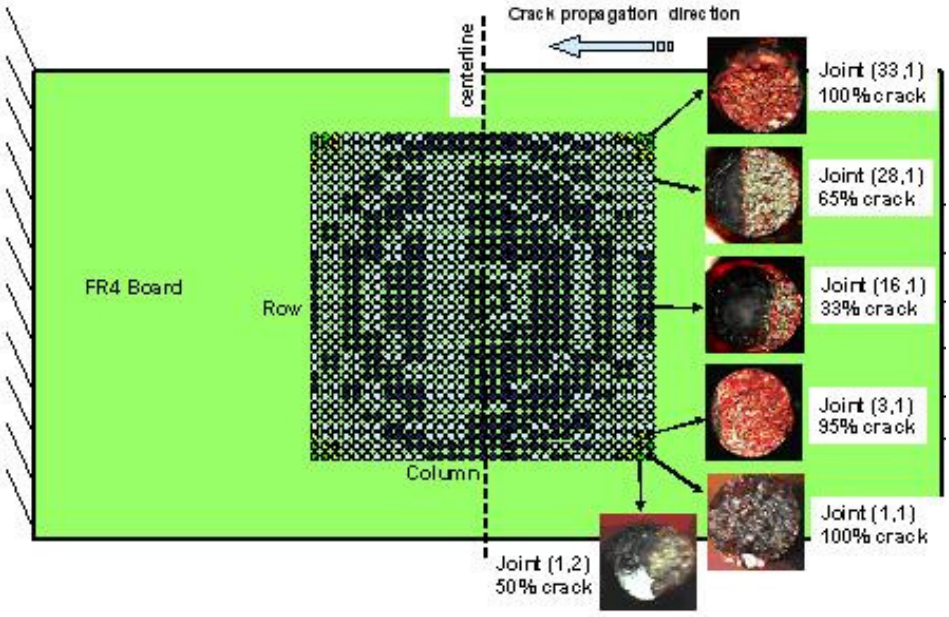


Figure 8-7. Dye and pry analysis of showing crack growth and distribution

The outermost joints, (1,1) and (33,1) , of the 33x33 solder joint array as notated in Figure 8-7 are seen to have the largest cracks and the greatest distribution of cracks. This is to be expected as the radius of curvature of the FR4 board is largest at the outermost joints as found previously by the authors in [63], and thus the stresses on these solder joints will be highest. For example, solder joint (1,1) in the outermost column has a 100% crack length, whereas the solder joint (1,2) in the next closest inner column has a crack length of only 50%. From Figure 8-7 it can also be seen that crack initiation in each solder joint occurred at the side of the solder joint closest to the clamped-clamped boundary conditions and propagated towards the centerline of the package. The predicted high stresses in the corner joints shown in Figure 8-5 agrees well with the failed corner joints seen in Figure 8-7. Additionally, the innermost solder joints in columns 8 thru 25 experience low stresses which agrees with the zero crack initiation in the dye-and-pry analysis.

The joints that failed in the vibration test have failures typical of brittle fatigue as the high strain rate under vibration testing does not allow creep damage to occur [81]. The joints

that failed from pull off of the ceramic substrate have a typical cone/cup fracture for ductile materials[78] as shown in Figure 8-8.

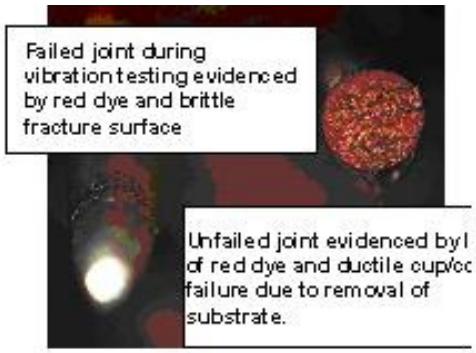


Figure 8-8. Ductile cup/cone failure of solder joints due to substrate removal vs. brittle failure due to vibration fatigue.

Dye-n-pry analysis was attempted for the single step ATC test vehicles and the sequential tests. However, the data did not reveal any conclusive information. The extreme deformation in the solder column under thermal cycling made it difficult to distinguish where the dye had penetrated into the solder column.

8.4. SOLDER JOINT FAILURE MECHANISM AND MICROSTRUCTURAL ANALYSIS

The dye-and-pry analysis reveals the amount of damage in various solder joints due to vibration testing, and as a next step, cross-sectional analysis was done to understand the nature of crack propagation in those joints that failed.

For vibration loading, the cracks occurred predominantly on the FR4 board side in the 90Pb10Sn column at the end of the 63Sn37Pb fillet as shown Figure 8-9a. To a lesser extent, some cracks occurred in the middle of the 90Pb10Sn column where the cross-sectional area happened to be smallest and axial stresses would be largest. The failure mode and location is consistent with similar findings elsewhere in the literature [52].

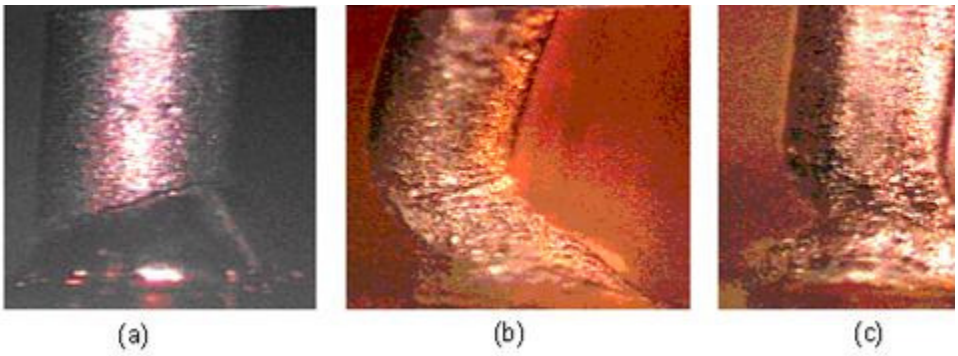


Figure 8-9. Fatigue of CCGA column under: (a) vibration loading. Note column is not distorted and no necking. (b,c) thermal cycling. Observe deformation and necking of 90PB10Sn column at 63Sn37Pb fillet.

Under thermal cycling, significant deformation of the column occurs due to the large CTE mismatch between the ceramic substrate and FR4 board as shown in Figure 8-9b. Necking of the fillet can also be seen under thermal cycling in Figure 8-9c.

Figure 8-10a shows a virgin CCGA solder column that has not been subjected to any environmental testing. By observing Figure 8-10b, it can be seen that there is very little distortion and microstructural changes under vibration loading. However, in contrast, as seen in Figure 8-10c, microstructural changes such as grain growth and dissolution of solders into other interfaces occurs under thermal cycling [81, 120].

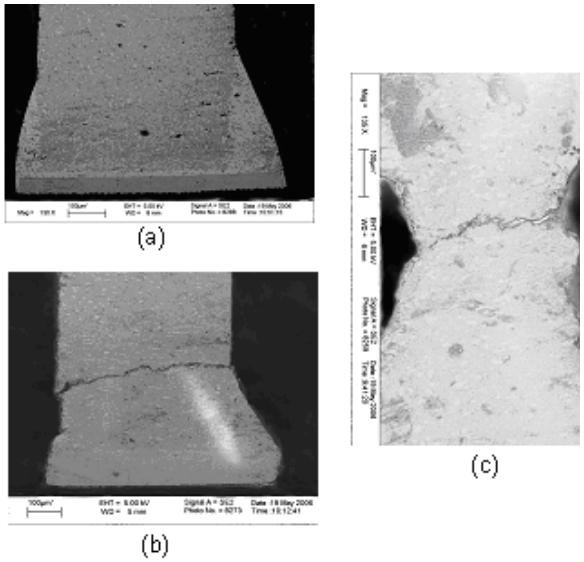


Figure 8-10. Cross-section scanning electron microscopy images of (a) virgin sample, (b) vibration failure, and (c) ATC failure

There are two stages to the development of a crack in solder; the first stage is crack initiation, and the second stage is crack propagation to failure. The amount of time spent in crack initiation and crack propagation is dependent upon the type and severity of loading, the strain rate of loading, creep characteristics of the solder, and the temperature of loading. For low cycle and low strain rate thermo-mechanical loading, crack initiation occurs quickly due to intergranular creep by grain boundary sliding that initiates cavities and cracks rather quickly [81, 120]. Darveaux shows that crack initiation under thermo-mechanical loading occurs in the first 10% of the fatigue life [20]. Zhang et al. observed for area array packages that the crack initiation period is brief compared to the crack growth period [135]. Once the crack is initiated, the rest of the life is spent in crack propagation [81].

For high cycle vibration fatigue the majority of the time may also be spent in crack propagation. At high frequency loading rates ($\dot{\varepsilon} > 0.02^{s-1}$) and low temperatures, the creep damage by intergranular grain boundary sliding does not occur as the grain boundaries are viscous, and the flow behavior then reflects the properties of the matrix boundaries [120]. In the case of a solder alloy such as 90Pb10Sn solder, micro cracks are initiated at phase boundaries resulting in phase separation, or at stress concentration locations where local plastic strains dominate and initiate cracks as shown in Figure 8-11. The micro cracks then grow in the Pb matrix until they coalesce with other micro cracks and eventually form a macro crack. Due to the elastic and low stress nature of high cycle fatigue, it may take a while to propagate a micro crack through the Pb matrix. Therefore crack propagation will be slow, unless a large number of micro cracks are initiated and form quickly into one macro crack. Figure 8-11 shows a vibration failure from test vehicle C where failure occurs in the 90Pb10Sn column. Microcracks can be seen to be forming at phase boundaries, propagating through the Pb matrix, and coalescing into a macro crack. In addition, it is likely that micro cracks were initiated at the radius of the 63Sn37Pb fillet and 90Pb10Sn column.

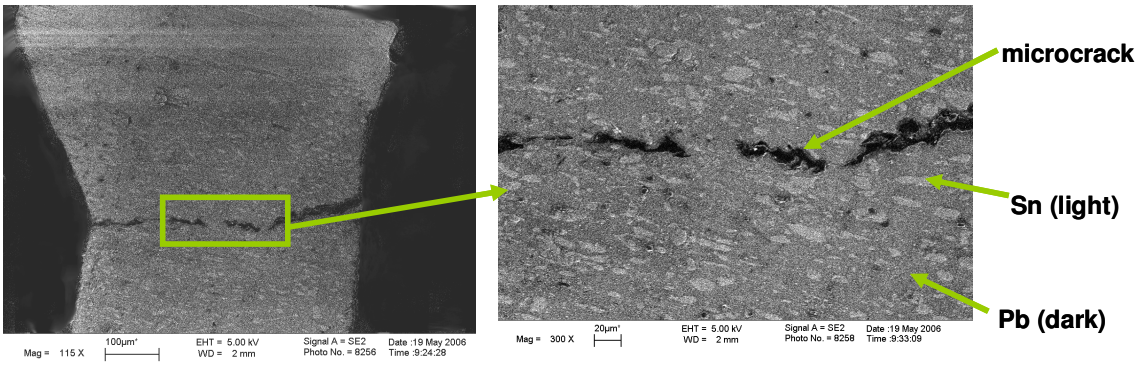


Figure 8-11. SEM images of high cycle fatigue crack in 90Pb10Sn column.

8.5. FATIGUE LIFE PREDICTION FOR 90PB10SN SOLDER UNDER VIBRATION LOADING

A fatigue life prediction equation was developed for 90Pb10Sn solder joints using the experimental data and the FEM. In this equation, the fatigue life of 90Pb10Sn solder joints was determined as a power-law function of the stress amplitude. A Weibull distribution for the experimental data is used in order to find the mean fatigue life. The experimental mean fatigue life is then related to the stresses calculated from the FEM. The following sections present the development of the stress-based predictive equation:

8.5.1. Weibull Distribution.

The Weibull distribution is often used to fit the distribution of solder joint fatigue life in electronic packages. Equation (8.3) is the Weibull cumulative failure distribution function:

$$F\%(N) = 1 - e^{-\left(\frac{N}{\alpha_w}\right)^{\gamma}} \tag{8.3}$$

where: N is the fatigue life (in cycles) of interest, $F\%(N)$ is the percent failed at cycles N, α_w is the characteristic fatigue life defined by failure of 63.2% of components, and γ is the shape parameter.

Figure 8-12 gives the characteristic fatigue life, α_w, and the shape parameter, γ, of the Weibull distribution for daisy chain R_0, R_1, and R_{XX}. The shape parameter γ values of

daisy chain rings R_0, R_1, and R_{XX} were 1.40, 1.50, and 2.11 respectively The relatively low values for the shape parameter γ indicate a large spread in the data and agree with other literature data on high cycle vibration of area array packages [62]. The characteristic fatigue life, N_{63}, of daisy chains R_0, R_1, and R_{XX} were 3.51E5, 5.44E5, and 2.07E6 respectively.

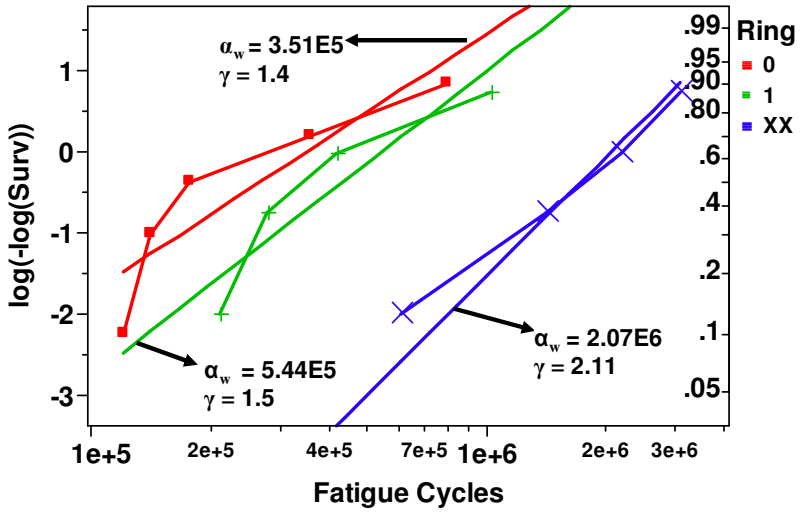


Figure 8-12. Weibull Fit of Fatigue data for 1.0Gin at natural frequency of test vehicles.

Now that α_w, and γ are known for each daisy chain ring, the mean fatigue life, N_{50}, can be found by using Eq. (8.3) and using a value of 0.5 for *F%(N)*. The mean fatigue life N_{50} will be used for development of a stress based prediction equation. Figure 8-12 shows the values for α_w, γ, and N_{50} for each daisy chain ring.

8.5.2. Power-Law Predictive Equation Based on Stress Amplitude.

As seen previously in Figure 8-5, each solder joint experiences different stresses under the same input acceleration due to bending of the board. A predictive fatigue equation which directly relates the solder joint stress to fatigue life has the greatest flexibility in predicting fatigue life for a variety of boundary conditions, input accelerations, and CCGA component sizes. Under vibration loading, as discussed earlier, the stresses in the solder fall within the elastic regime, and therefore, high-cycle fatigue conditions apply.

Traditionally, the high cycle fatigue life is obtained from the stress amplitude [78] as in equation (8.4):

$$\sigma_a = \sigma_f^{'} \left(2N_f\right)^b \tag{8.4}$$

where, σ_a is the stress amplitude in MPa, $\sigma_f^{'}$ is the fatigue strength coefficient in MPa, b is the fatigue strength exponent, and N_f is the number of cycles to failure and is taken to be the value at N_{50}.

A commonly used value for the fatigue strength exponent, b, for 63Sn37Pb solder is -0.25 [55]. The only published fatigue strength exponent specifically for 90Pb10Sn was found in [136] and is given as -0.13. This value was obtained using low-cycle bending tests of CCGA's and may not be relevant to the high cycle fatigue in this study.. Therefore, we will develop our own constants for high cycle (>10^5 cycles) fatigue of 90Pb10Sn solder.

A regression analysis on Eq. (8.4) to determine the constants $\sigma_f^{'}$ and b will minimize error on the response σ_a, however the goal is to predict N_f and minimize error on N_f. Therefore, Eq. (8.4) will be rearranged into Eq. (8.5) so that N_f is the response variable.

$$N_f = C_1\left(\sigma_a\right)^n \tag{8.5}$$

where C_1 equals $\frac{1}{2}\left(\frac{1}{\sigma_f^{'}}\right)^{1/-b}$ and n equals $1/-b$.

Constants will be developed for $\sigma_f^{'}$ and b depending on the definition of σ_a and whether the detailed solid model or the equivalent beam model in the FEM were used for the solder joints at locations J_0, J_1, and J_{XX}. The first definition of σ_a is based on a volume-averaged VonMises stress amplitude taken from the detailed solid model as shown equation (8.6). The detailed solid model will allow for investigation of the effects of solder joint geometry, such as joint diameter and solder paste volume, on vibration fatigue life.

$$\sigma_a = \frac{\sum_{i=1}^{\#elements} \sigma_{vm}^{i} \cdot V^{i}}{\sum_{i=1}^{\#elements} V^{i}} \tag{8.6}$$

where V^i is the volume of element i in mm^3, and σ^i_{vm} is the equivalent VonMises stress of element i calculated according to equation (8.7).

$$\sigma_{vm} = \frac{1}{\sqrt{2}}\left(\sqrt{(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_x)^2 + 6(\tau_{xy}^2 + \tau_{yz}^2 + \tau_{zx}^2)}\right) \tag{8.7}$$

where σ_x, σ_y, and σ_z are the normal stresses in MPa, and τ_{xy}, τ_{xy}, and τ_{xz} are the shear stresses in MPa.

While the vonMises stress is used in this study, it may be possible to consider individual stress components and determine failure based on a multiaxial fatigue criteria [137]. For example, the shear stress distrubtion on solder joints may be different then the axial stress distribution shown in Figure 8-5 and may be a better indicator of which joints fail under a different loading or at a different fundamental frequency.

The stresses are volume averaged over two separate layers of solid elements as shown in Figure 5-1, one layer is on the board side and the other layer is at the substrate side. The layer with the highest volume averaged VonMises stress amplitude is used in the fatigue equation. Figure 8-13 shows a plot of the VonMises stresses in the two volume-averaged layers of the J_0 solder joint under a 1.0G sinusoidal acceleration driven at the f_n of 308Hz.

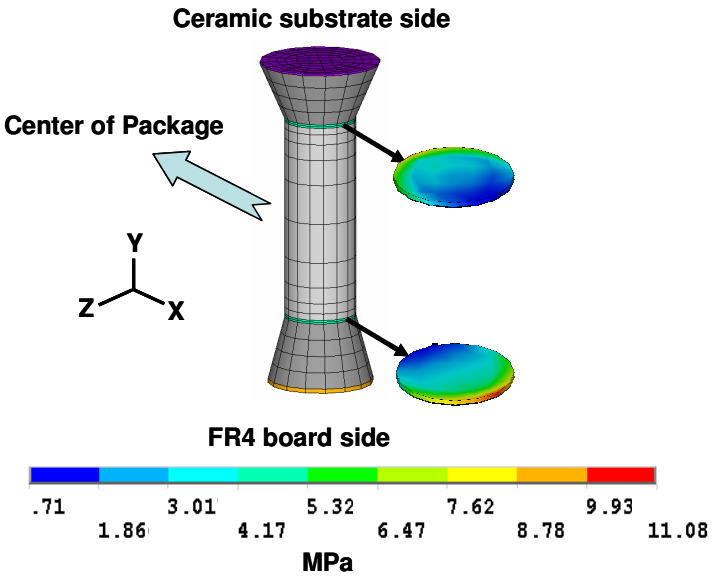


Figure 8-13. Vonmises stresses for J_0 solder joint under a 1G sinusoidal acceleration driven at the f_n of 308Hz.

From the harmonic FEM analysis of CCGA package assemblies, the stress amplitude for each ring was obtained and plotted against N_f as shown in Figure 8-14.

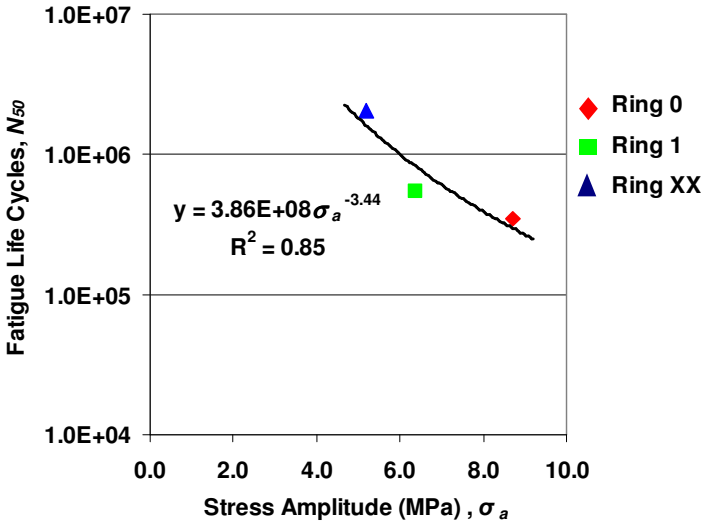


Figure 8-14. Plot of N_{50_exp} versus σ_a for each daisy chain ring.

Using regression analysis for Eq. (8.5) the constants σ'_f and b were 383 MPa and -0.29 for the detailed solid model. It is worth noting that the value of b of -0.29 for the

90Pb10Sn solder in the detailed model is close to the value of -0.25 traditionally used for 63Sn37Pb.

Substituting the values $\sigma_f^{'}$ and b into Eq. (8.5) leads to Eq. (8.8) for estimation of fatigue life using the detailed solid model.

$$N_f = 3.86E08(\sigma_a)^{-3.44} \tag{8.8}$$

8.6. VALIDATION OF PREDICTIVE MODELS

The developed predictive models were validated using various test cases and are summarized in the following sections.

8.6.1. Vibration Fatigue Life Mapping for an Area-Array Package

The developed predictive Eq. (8.8) is based on three daisy chains from five test vehicles. As the dye-and-pry technique provided information on the crack propagation across all of the solder joints, Eq. (8.8) was validated against the results from the dye-and-pry analysis. Accordingly, a normalized fatigue life distribution of every solder joint in the CCGA is shown in Figure 8-15. Figure 8-15 is obtained by substituting the equivalent beam stress amplitudes from Figure 8-5 into Eq (8.8) and normalizing the values to the minimum fatigue life.

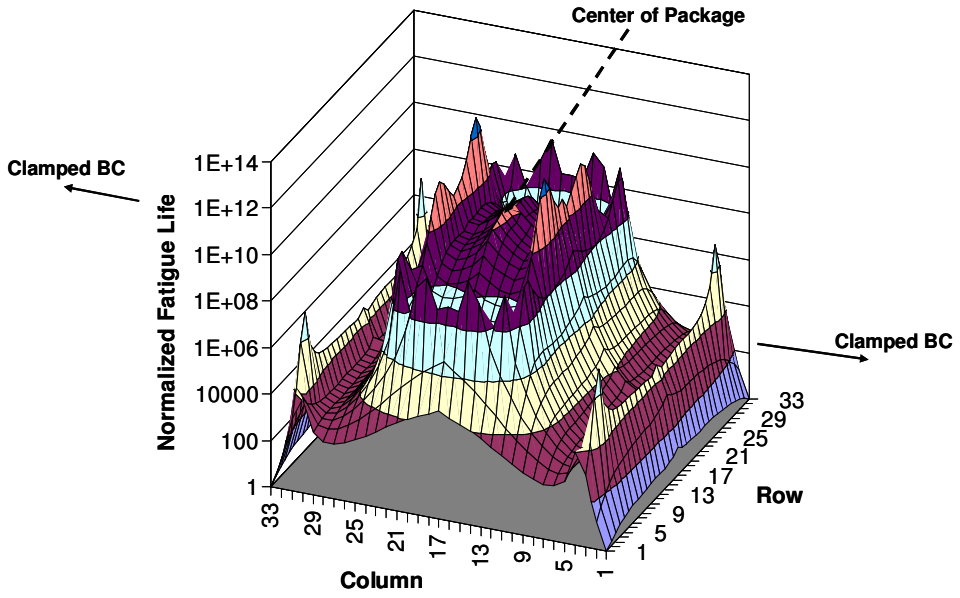


Figure 8-15. Normalized Fatigue Life for CCGA solder joint array based on input acceleration G_{in} of 1G

It can be observed in Figure 8-15 that the solder joints closest to the clamped-clamped boundary conditions in Row 1 and Row 33 have the shortest fatigue life, which is consistent with the dye-n-pry results. Furthermore, as one traverses from the clamped edge toward the center of the package, the fatigue life gradually increases, as seen in the dye-and-pry analysis where the magnitude of crack propagation continues to decrease. Near the center of the die, the fatigue life is several orders of magnitude higher than the corner solder joints, and therefore, such joints are least likely to fail under vibration loading with clamped-clamped boundary conditions. This observation was also validated through dye-and-pry analysis where the solder joints near the center did not show any crack.

Based on the fatigue life map presented in Figure 8-15, the life of a full area array electronic package with clamped-clamped boundary conditions under vibration loading component can be improved two to three orders of magnitude, if one were not to use the corner solder joints for critical electrical connections.

8.6.2. Heat Sink Effect on the Vibration Fatigue Life..

As a second case, the developed approach was validated using experimental vibration failure data obtained from a CCGA package with a heat sink. The developed FEM and Eq. (8.8) will enable prediction of solder joint fatigue life for a CCGA electronic component with any boundary condition under vibration loading. Several 'what-if' analyses can be quickly done to assess the reliability under vibration loading. Accordingly, experimental vibration testing was conducted on a CCGA package assembly with a 100g copper mass attached to the package. The copper mass was attached to mimic the presence of a heat sink on the package. The natural frequency was measured to be 182 Hz, and the decrease in the natural frequency from 308 Hz to 182 Hz is due to the presence of 100g mass on the package. The input acceleration was set to 1.0G at its natural frequency f_n of 182Hz, and the fatigue life of the daisy chain R_{xx} was found to be 61,800 cycles.

Using the finite-element model developed, σ_a was found to be 12.2 MPa which translates to a predicted N_{50} of 70,700 cycles for daisy chain R_{XX} using equation (8.8). Thus, the predicted N_{50} life using equation (8.8) is within 15% of the experimental fatigue life and is acceptable, especially for high-cycle fatigue where the life can be in the millions of cycles and the scatter in data is high. When compared against the fatigue life of a CCGA without a heatsink, it is seen that the addition of a 100g heatsink to the CCGA decreases the solder joint fatigue life by 67%. This finding is similar to the finding from a separate study by Cole et al. [52, 138] in which the effect of heatsink mass on solder joint fatigue life for CCGA's under random vibration testing was studied.

8.6.3. Solder Joint Life Prediction for Sinusoidal Sweep Tests.

Sinusoidal vibration tests such as Bellcore TR-NWT-000063 that sweep across a range of frequencies either logarithmically or linearly are more common than the fixed frequency test discussed thus far. Therefore, the developed model was used to predict the fatigue

life under such sinusoidal sweep test and was validated using experimental data. The fatigue life under frequency sweep tests can be predicted using, for example, a cumulative damage rule such as Miner's Cumulative Damage Rule as shown in Eq. (8.9) for a linear sweep rate.

$$CDI = N_{sw} \sum_{i=1}^{\substack{\#increments \\ per\ sweep}} \frac{n_i}{N_i} = N_{sw} \sum_{i=1}^{\substack{\#increments \\ per\ sweep}} \frac{\frac{1}{R_s}\left(f^2{}_i - f_{i-1}^2\right)}{N_i} \tag{8.9}$$

where *CDI* is the cumulative damage index, N_{sw} is the number of sweeps defined as a pass up and down the frequency range of interest, n_i is actual number of cycles for the i^{th} increment, N_i is the predicted number of cycles to failure for the i^{th} increment, obtained using equation (8.9), R_s is the linear sweep rate (Hz/sec), and f_i is the end frequency for the i^{th} increment. *CDI* ranges from 0 to 1.0 with 0 being the undamaged state and 1.0 being the fully damaged state. Failure is typically defined when the CDI exceeds a critical value of 0.7 [55].

The number of sweeps N_{SW} to failure can be found by rearranging Eq. (8.9) into Eq. (8.10).

$$N_{sw} = \frac{CDI}{\sum_{i=1}^{\substack{\#increments \\ per\ sweep}} \frac{n_i}{N_i}} = \frac{CDI}{\sum_{i=1}^{\substack{\#increments \\ per\ sweep}} \frac{\frac{1}{R_s}\left(f^2{}_i - f_{i-1}^2\right)}{N_i}} \tag{8.10}$$

The total number of cycles to failure can be found using Eq. (8.11)

$$\text{Total } N_{50} \text{ to failure} = N_{SW} \times R_s \times 2\Delta f \times f_n \tag{8.11}$$

where N_{sw} is the number of sweeps defined as a pass up and down the frequency range of interest, R_s is the linear sweep rate (Hz/sec), Δf is the frequency range to be swept in one pass, and f_n is the natural frequency to be swept around.

Most of the damage will occur as the frequency is swept between the half power points where the peak response occurs [55]. Thus, at least three increments should be used in

this range to capture the peak response and the half-power points. Greater accuracy may be obtained by using more increments.

For example, sweep testing was conducted using a CCGA test vehicle assembly, as shown in Figure 8-1, and sweeping it over a frequency range of Δf ±30Hz around the natural frequency f_n of 307 Hz with an input acceleration of 1G. Figure 8-16 shows the FEM stress amplitude response of solder joint J_{xx} used to characterize daisy chain ring R_{xx} of the CCGA. There are nine increments, i=9, over the frequency range from 277Hz to 337Hz in which the stress amplitude σ_a is calculated using the finite-element model and then used in Eq. (8.8) to calculate N_i . The grayed out regions represent the half-power point region where the majority of damage is accumulated. Using Eq. (8.11) with a *CDI* of 1.0 along with Eq. (8.8), the predicted number of sweeps N_{SW} was 7.9 and the total N_{50} cycles to failure is 2.9E6. During the experimental sweep test, it was found that N_{SW} was 7.4 and the total N_{50} cycles to failure was 2.1E6, resulting in a 7% difference between the predicted and experimental total N_{50} cycles to failure.

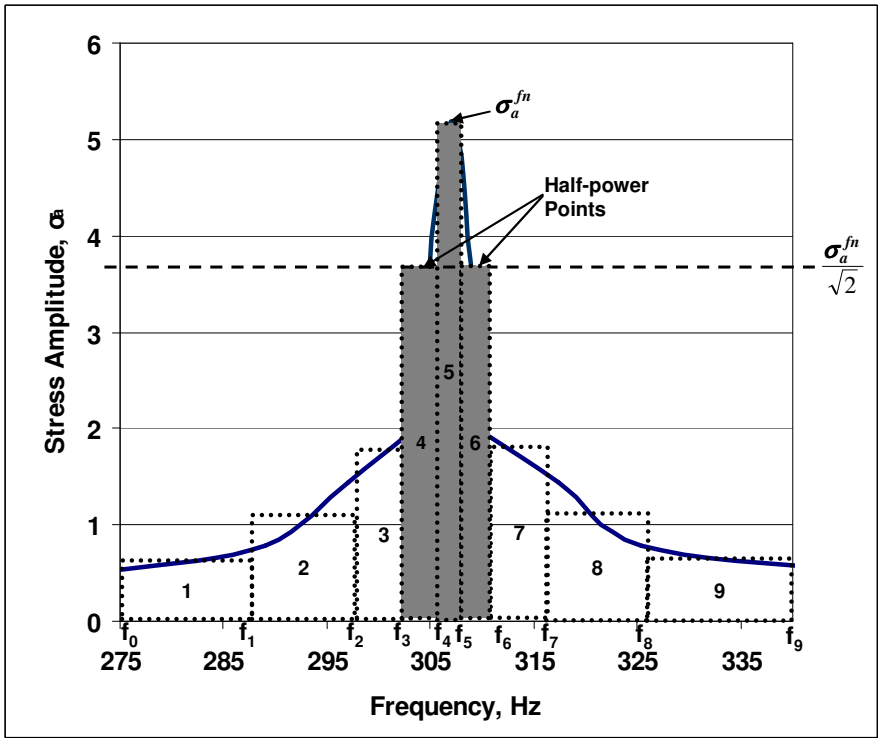


Figure 8-16. Increments for predicting fatigue life by Miner's Rule

8.7. DISCUSSION ON VALIDATION

In general, it is seen that the developed approach can map the solder behavior across an area array of interconnects. Also, it can be used to determine the fatigue life of solder joints under a wide range of geometries including the addition of heat sinks. Furthermore, the proposed model can be used to determine solder joint fatigue life under vibration sweep tests. In addition to such validations, the proposed model and approach can be used to develop certain design recommendations. For example, based on the results obtained for the area-array of interconnects, it can be said that the corner joints undergo early fatigue failure under vibration loading with clamped-clamped boundary conditions, and therefore, it is recommended that the corner joints be removed or used with redundant joints to reduce the chances for early fatigue failure under vibration loading (as well as thermo-mechanical loading). As the addition of heat sink reduces the vibration fatigue life, it is recommended that the heat sink does not exceed a mass of 100g for a CCGA with 1089 interconnects. Furthermore, the maximum damage occurs near the natural frequency of the system, and therefore, it is recommended that the natural frequency be increased or changed so that such a frequency is not experienced during operation.

8.8. CHAPTER SUMMARY

Through numerical FEM models and experiments, the high cycle solder joint fatigue life for 90Pb10Sn solder in a CCGA electronic component was determined. The location of solder joint failures was identified through dye-n-pry analysis and correctly predicted with the numerical FEM. The solder joints close to the clamped boundaries experience the greatest stress amplitude and fail first. The mechanism of failure was observed to be microcrack initiation at phase boundaries followed by microcrack coalescence into macrocracks. The fatigue life of a CCGA can be greatly enhanced by not using the solder joints closest to constrained boundary conditions for electrical purposes. A stress based predictive fatigue life equation for 90Pb10Sn solder was developed and was

applied to predict solder joint fatigue life under frequency sweep as well as under heat sink attachment. The developed stress based predictive fatigue life equation can be used for several 'what-if' analyses without costly and time-consuming experiments being performed. The methodology, developed in this work, has the potential for application for other packages as well as for lead-free solder alloys.

CHAPTER 9

DEVELOPMENT OF UNIVERSAL PREDICTIVE FATIGUE LIFE EQUATION AND STUDY OF THE EFFECT OF DESIGN PARAMETERS

9.1. INTRODUCTION

In the foregoing chapters, a finite-element based approach was presented to predict the solder fatigue life under various loading conditions. To be able to use such a model, it is necessary for the user to have a good understanding of finite-element analysis and mechanics of materials. The solder damage parameter, Ψ, determined using the finite-element technique is highly dependent upon numerical modeling and material property assumptions [139], such as: (1) Material modeling assumptions: i.e., plasticity, creep, temperature dependency, (2) Mesh Characteristics: Element type, singularity, and mesh density, and (3) Type of analysis: Plane Strain, Plane Stress, 3D [129]. Thus, for a given package and under given loading conditions, two independent researchers may not report the same predicted result. For example, researchers in the past who have assessed CBGAs with the dual melt solder ball structure and presented detailed modeling and experimental results are Corbin [13], Martin et al. [127], Vandevelde et al. [112], Li and Mahajan [140], Hong and Yuan [30], Pang et al. [141], Perkins and Sitaraman [142, 143], Wong et al. [6], Xie and Wang [144], and Burnette et al. [145]. No two researchers have consistently used the same FEM assumptions or material models/properties. Even if the same fatigue life equation was used, such as Engelmaier's [45] modified Coffin-Manson equation, the predicted fatigue lives are different due to differences in modeling and material assumptions.

To be able to address these concerns with the traditional finite-element and predictive equation approach, this thesis aims to develop a universal polynomial predictive equation that is independent of material, geometry, meshing, and other assumptions. Accordingly,

this thesis aims to use a Design of Simulation (DOS), an analysis of variance (ANOVA), and regression analysis to develop a universal predictive fatigue equation for a given family of electronic packages for the use of the electronic packaging community at large. Thus, the damage-metric based equation in Eq. (4.7) is transformed into a universal equation for any temperature cycle and failure percentage:

$$N_{50} = C_1(\Psi)^n \overset{regression}{\underset{analysis}{\Rightarrow}}$$

$$N^{ATC} = \left(\frac{\ln(1-F\%\times.01}{\ln 0.5}\right)^{\frac{1}{\gamma}} \times \left(\frac{\Delta T^{DOS}}{\Delta T^{ATC}}\right)^{1.9} \left(\frac{f^{ATC}}{f^{DOS}}\right)^{1/3} \left(e^{1414\left(\frac{1}{T_{peak}^{ATC}}-\frac{1}{T_{peak}^{DOS}}\right)}\right) \times \left[\sum_{k=0} \beta_k X_k\right] \tag{9.1}$$

where $F\%$ is the percent failure of the population, ΔT is the temperature range in Kelvin, f is the frequency of cycles in cycles per hour, T_{peak} is the peak temperature in Kelvin, β_k are regression coefficients, and X_k are design variables. The superscript *ATC* refers to the new desired ATC, and the superscript *DOS* refers to the simulated thermal cycle in the DOS.

The proposed universal predictive fatigue equation (1) combines the strength and the results of analytical, numerical, and experimental techniques, (2) removes the inconsistencies or disparities brought about by different researchers, (3) does not require mature understanding of mechanics, numerical models, material behavior, etc. (4) uses Coffin-Manson type equation underneath its development, however masks such equations from the user's viewpoint. Although this chapter demonstrates the approach for CBGAs, similar universal predictive equations can be developed for PBGA and chip-scale packages with appropriate numerical models and experimental data. Therefore, CBGAs should be treated as one example case for the proposed methodology.

9.2. METHOD

Table 9-1 outlines the steps involved in the development of the universal predictive fatigue equation. Such a universal predictive fatigue equation will facilitate designers to

determine the solder joint fatigue life for a wide range of parameters for a given family of microelectronic packages without running experiments or finite-element models.

Table 9-1. Steps to derive the universal predictive fatigue life equation

Step	Description	Outcome	
1	Experimental ATC tests to determine the solder joint fatigue reliability. Literature data used. See Table 1A.	$N50_{exp}$	Traditional Approach
2	Analytical/Numerical Modeling	Ψ, Damage Parameter	
3	A Coffin-Manson (CM) type non-linear equation is derived to relate damage parameter from numerical analysis to the mean fatigue life from experiments. Two or more sets of experimental data are required to determine the constants.	$N_{50} = a/\left(K_3(\Psi)^{K_4}\right)$	
4	Design parameters important to solder joint fatigue under ATC are identified. Also, the range of variation for these parameters is identified.	$A_1 \leq A \leq A_2$, $B_1 \leq B \leq B_2$	Proposed Approach
5	A full factorial Design of Simulations (DOS) is performed for the design parameters from Step 4, the damage parameter per cycle identified, and the fatigue life is then calculated using the equation from Step 3.	N_{50} for DOS	
6	An ANOVA and linear regression analysis is performed to develop a linear regression equation between the fatigue life and the design parameters.	Effects of Design Parameters $N_{50} = g(A,B,C,..)$	
7	The linear regression equation is then augmented with the Norris-Landzberg acceleration factor (AF) so that the equation can be used for any thermal cycling condition. Package-specific Weibull distribution function is also added to the equation so that the number of cycles to failure for 1%, 63.2% or any % failure can be determined.	N^{ATC} for any thermal environment and failure percentage	
8	Uncertainty analysis is performed to account for uncertainty in the error of the regression analysis, the Norris-Landzberg AF, and the Weibull distribution. The combined uncertainty, u_{N_ATC} is used to estimate a Confidence Interval (CI), $N^{ATC} \pm k u_{N\_ATC}$	$N^{ATC} \pm k u_{N\_ATC}$	

According to Table 9-1. Steps to derive the universal predictive fatigue life equation. The first three steps have been covered in previous chapters. Chapter 5 discussed the development of a unified finite-element model, and Chapters 6 and 7 discussed the development of fatigue-life prediction equation and the validation of the finite-element model. The total strain energy density based equation (7.2) is used to predict the mean fatigue life N_{50} using the unified FEM. The following sections discuss the remaining steps in the development of the universal polynomial predictive equation.

9.2.1. Steps 4 and 5: Design of Simulations (DOS)

Prior to the development of universal equation, it is necessary to determine the parameters that are of primary interest for the packaging engineers, and use such parameters to develop the universal equation for predicting solder joint fatigue life. Based on talking to industry experts and literature review, it appears that the following design parameters are of interest: substrate size, CTE mismatch, substrate thickness, board thickness, and solder joint pitch. Accordingly. the effects of the following design parameters on solder joint fatigue life have been studied: substrate size (*A*) ranging from 25mm to 32.5mm square, CTE mismatch between the ceramic substrate and board (*B*) ranging from 7.4 to 11.2 ppm/K, substrate thickness (*C*) ranging from 0.8 to 2.9 mm, board thickness (*D*) ranging from 1.57 to 2.8 mm, and joint pitch (*E*) ranging from 1 to 1.27 mm on solder joint fatigue life. The range of values chosen are indicative of common values used for CBGA's with 32.5x32.5mm substrate sizes and smaller. A full 2-level, 5-factor DOS (2^5 = 32 runs) was performed. For each of the 32 cases shown in Table 9-2 a finite-element simulation was performed, total strain energy density per cycle, ΔW_{tot} is identified, and N_{50} is then determined from Eq. (7.2). The simulated ATC cycle was -25/110°C at 2cph.

Table 9-2. Design of simulation (DOS) and predicted N_{50} for CBGA under ATC

RUN	*A* (mm)	*B* (ppm/K)	*C* (mm)	*D* (mm)	*E* (mm)	ΔW_{tot}	N_{50} using Eq. (7.2).
1	25.0	11.2	2.9	2.80	1.27	0.0861	603
2	25.0	11.2	2.9	1.57	1.27	0.0810	652
3	25.0	11.2	2.9	2.80	1.00	0.0670	774
4	25.0	11.2	2.9	1.57	1.00	0.0623	849
5	25.0	11.2	0.8	2.80	1.27	0.0518	1158
6	25.0	11.2	0.8	2.80	1.00	0.0414	1438
7	25.0	11.2	0.8	1.57	1.27	0.0425	1494
8	25.0	7.4	2.9	2.80	1.27	0.0389	1672
9	25.0	7.4	2.9	1.57	1.27	0.0375	1754
10	25.0	11.2	0.8	1.57	1.00	0.0351	1776
11	25.0	7.4	2.9	2.80	1.00	0.0300	2176
12	25.0	7.4	2.9	1.57	1.00	0.0288	2295
13	25.0	7.4	0.8	2.80	1.27	0.0274	2622

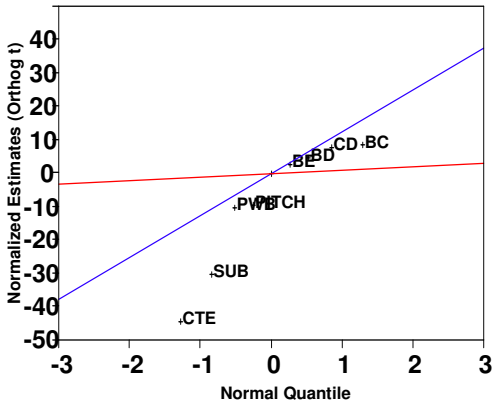
RUN	*A* (mm)	*B* (ppm/K)	*C* (mm)	*D* (mm)	*E* (mm)	ΔW_{tot}	N_{50} using Eq. (7.2).
14	25.0	7.4	0.8	2.80	1.00	0.0229	3085
15	25.0	7.4	0.8	1.57	1.27	0.0211	3663
16	25.0	7.4	0.8	1.57	1.00	0.0186	4012
17	32.0	11.2	2.9	2.80	1.27	0.0904	566
18	32.0	11.2	2.9	1.57	1.27	0.0839	623
19	32.0	11.2	2.9	2.80	1.00	0.0694	739
20	32.0	11.2	2.9	1.57	1.00	0.0638	824
21	32.0	11.2	0.8	2.80	1.27	0.0511	1179
22	32.0	11.2	0.8	2.80	1.00	0.0413	1443
23	32.0	11.2	0.8	1.57	1.27	0.0425	1491
24	32.0	7.4	2.9	2.80	1.27	0.0387	1685
25	32.0	7.4	2.9	1.57	1.27	0.0373	1764
26	32.0	11.2	0.8	1.57	1.00	0.0350	1783
27	32.0	7.4	2.9	2.80	1.00	0.0303	2145
28	32.0	7.4	2.9	1.57	1.00	0.0290	2270
29	32.0	7.4	0.8	2.80	1.27	0.0268	2701
30	32.0	7.4	0.8	2.80	1.00	0.0227	3104
31	32.0	7.4	0.8	1.57	1.27	0.0209	3719
32	32.0	7.4	0.8	1.57	1.00	0.0186	4014

9.2.2. Step 6a: Analysis of Variance (ANOVA)

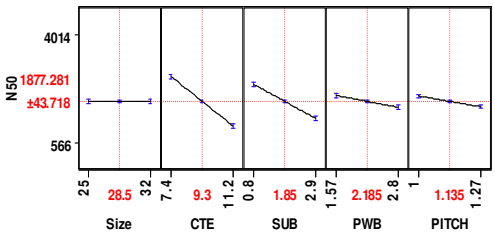
An ANOVA analysis will help determine the predictors that have a significant effect on the response. *N50* is the response and the factors are the Substrate Size (*A*), CTE Mismatch (*B*), Substrate Thickness (*C*), Board Thickness (*D*), and Pitch (*E*). JMP 5.1 [131] is used for all analyses.

Figure 9-1a shows a normal probability plot of the effects with a confidence interval of 90%. Those predictors that fall significantly away from the normal line are the influential predictors that significantly affect the response, and accordingly, the influential predictors are found to be in the order of importance: *B, C, D, E, BC, CD, BD, BE*. Also, from Figure 9-1b it is seen that for the selected range of values, change in the values of predictors *B, C, D*, and *E* result in a corresponding change in N_{50}, and thus, the influential predictors are *B, C, D,* and *E* in that order. Beyond the individual predictors, the interaction effects can be seen through Figure 9-1c. As seen in Figure 9-1c and Figure 9-1a, interaction effects are dominant *for BC, CD, BD*, and *BE* in that order. As

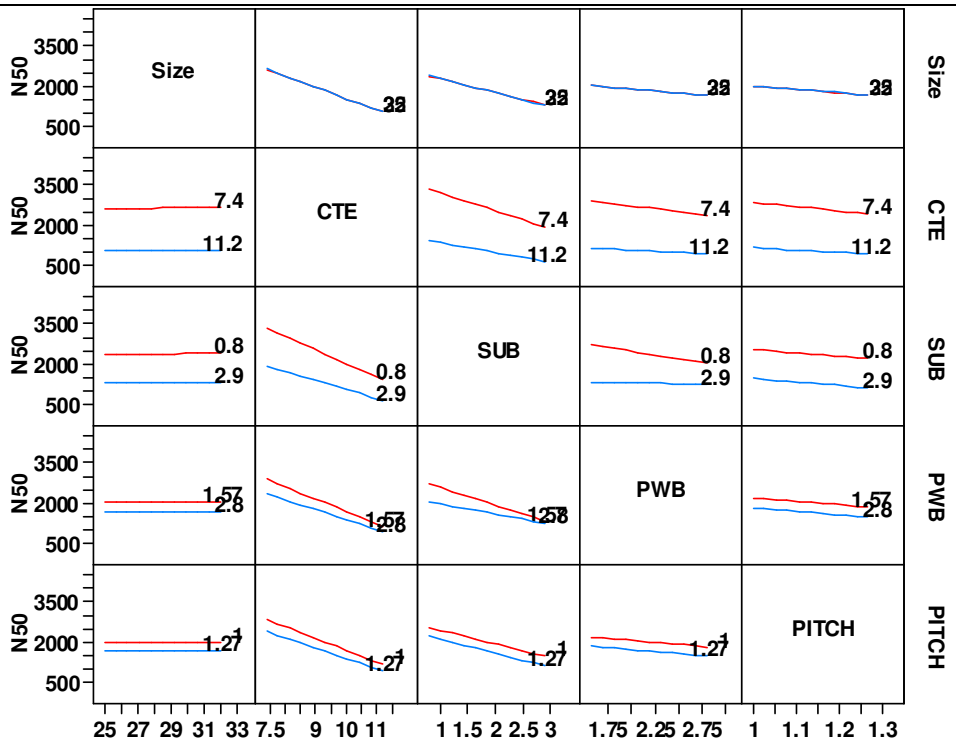
seen from Figure 9-1a, Figure 9-1b, Figure 9-1c, predictor *A*, either alone or in combination with other predictors, has minimal influence on the fatigue life. Additional discussion on the influence of *A* (substrate size) on fatigue life is presented in latter sections.



(a) Normal Plot



(b) Main Effects



(c) Interaction Effects

Figure 9-1. (a) Normal Probability Plot (b)Main Effects (c) Interaction Effects of DOS

9.2.3. Step 6b: Linear Regression

Now that we have determined the influential predictors on the response, we can develop a linear regression equation that relates the response to the predictors. The regression equation has an R_{sq} value of 0.99, indicating that the fit is acceptable. The C_p value of the regression analysis indicates the optimum number of terms to be used in the regression analysis and is equal to 8.85. Table 9-3 shows the estimated coefficients of various terms predictor terms and the associated standard error. The standard error is an estimate of the standard deviation for that term. The probability for the t-statistic, (Prob>|t|) is the probability of obtaining a value at least as extreme if that term were not in the regression. A probability for the t-statistic below 5% indicates that term is significant. Based on both the standard error and the probability for the t-statistic, it is seen that *A* (substrate size) has minimal influence on the fatigue life, which is consistent with the ANOVA results.

Table 9-3. Results of linear regression analysis

Term	Estimated Coefficients	Std Error	Prob>|t|
Intercept	12475.94	500.84	<.0001
Substrate Size (A)	0.24	5.87	0.9676
CTE Mismatch (B)	-719.91	44.25	<.0001
Substrate Thickness (C)	-1728.15	120.01	<.0001
Board Thickness (D)	-1380.65	177.06	<.0001
Pitch (E)	-1245.60	152.26	<.0001
CTE Mismatch x Substrate Thickness (BC)	78.74	10.30	<.0001
CTE Mismatch x Board Thickness (BD	72.45	17.59	0.0004
Substrate Thickness x Board Thickness (CD)	220.24	31.83	<.0001

Based on these considerations, the best regression is of the simple form

$$N_{50} = 12475 - 0.241A - 720B - 1728C - 1380D - 1246E + 78.74BC + 72.45BD + 220CD \qquad (9.2)$$

Although the ANOVA and regression analyses indicate the influence of the substrate size *A* on the solder joint fatigue life has minimal influence, the predictor term *A* is still included in the regression model for reasons explained later in this paper.

9.2.4. Step 7. Norris-Landzberg Acceleration Factor (AF) and Weibull Distribution

The regression model in Eq. (9.2) is for accelerated thermal cycling between -25°C and 110°C at 2 cph. To determine the N_{50} fatigue cycles for other ATC tests, the Norris-Landzberg equation [126]shown previously in Eq. (2.2), can be used to determine the *AF*.

In addition to different ATC conditions, it is also important to be able to determine the fatigue life for 1%, 63.2% and other percentage failures. For example, finding the solder joint fatigue life at a probability other than 50% is of interest for applications requiring high reliability such as medical and military applications where 1% fatigue failure is desired. A two-parameter Weibull analysis is used to predict the fatigue life at percentages other than the mean life at 50%, $N_{50,:}$

$$F\%(N) = 1 - e^{-\left(\frac{N}{\alpha_w}\right)^{\gamma}} \tag{9.3}$$

where: *N* is the fatigue life in cycles of interest, *F%(N)* is the percent failed at cycles *N*, α_w is the characteristic fatigue life defined by failure of 63.2% of components, γ is the shape parameter. The shape parameter varies depending upon the type of package and the quality of assembly; for CBGA, values for the shape factor gathered from literature data range between 4 and 11.

The two-parameter Weibull function has been shown to give very conservative estimates for prediction of fatigue lives at low probabilities [146]. A three-parameter Weibull distribution includes a failure-free life and may be more appropriate [146]. However, the determination of the failure free life is more difficult without experimental data. A lognormal distribution is also common for CBGAs [126]. It is more difficult to put in an

analytical solution as lookup tables or a numerical method must be used as there is no closed form solution for the cumulative failure distribution.

Eq. (9.3) is rewritten into a ratio of N^{ATC}/N_{50}^{ATC}. Rewriting Eq. (9.3) involves solving for the characteristic fatigue life, α_w, in terms of N_{50}, substituting α_w back into Eq. (9.3), and then rewriting Eq. (9.3) in terms of N^{ATC}/N_{50}^{ATC}. The final equation is shown in Eq. (9.4) and is called the *Weibull* factor.

$$Weibull = \frac{N^{ATC}}{N_{50}^{ATC}} = \left[\frac{\ln(1 - F\% \times 0.01)}{\ln 0.5}\right]^{\frac{1}{\gamma}} \tag{9.4}$$

By combining Eq.(2.2), Eq. (9.2), and Eq. (9.4), the final predictive fatigue equation for any accelerated thermal cycle at a given failure percentage, N_{ATC}, can be presented as a product of three functions

$$N^{ATC} = (Weibull) \times (AF) \times (N_{50}) = \left(\frac{N^{ATC}}{N_{50}^{ATC}}\right) \times \left(\frac{N_{50}^{ATC}}{N_{50}^{DOS}}\right) \times \left(N_{50}^{DOS}\right) \tag{9.5}$$

9.2.5. Step 8. Standard Uncertainty of the Prediction

Every prediction of fatigue life N^{ATC} using Eq. (9.5) will have some uncertainty associated with it due to the uncertainty of the constants in the *Weibull*, *AF*, and N_{50} factors. The method developed by NIST for reporting uncertainties *[147]* is used to assess how the uncertainties in the *Weibull*, *AF*, and N_{50} affect the combined uncertainty in predicting the fatigue life NATC.

In order to assess the uncertainty in Eq. (9.5), a combined standard uncertainty, u_{N_ATC}, along with a constant coverage factor, k, is used to give an expanded uncertainty, which is similar to a confidence interval (CI) [147] for each prediction:

$$N^{ATC} \pm k u_{N\_ATC} = (Weibull \pm u_{Weibull}) \times (AF \pm u_{AF}) \times (N_{50} \pm u_{N\_50}) \tag{9.6}$$

where: k is a coverage factor and is dependent upon a level of confidence, p. Typical values for the coverage factor based on a normal distribution are k= 1, 2, and 3 for level

of confidences p= 68.2%, 95.5%, and 99.7% respectively. $u_{Weibull}$, u_{AF}, and u_{N_50} are the standard uncertainties for the *Weibull* factor, *AF,* and N_{50} factors respectively.

The combined standard uncertainty u_{N_ATC}, was derived from the standard uncertainties, $u_{Weibull}$, u_{AF}, and u_{N_50}, using the law of propagation of uncertainty which is based on a first-order Taylor series approximation [147] as shown in Eq. (9.7). The correlation terms are dropped as the estimated uncertainties are assumed to be independent of each other.

$$u_c = \sqrt{\sum_{i=1}^{N}\left(\frac{\partial f}{\partial x_i}\right)^2 u^2(x_i)} \tag{9.7}$$

where: N is the number of terms in the function f, $\frac{\partial f}{\partial x_i}$ is the derivative of the function with respect to the term *xi*, and *u2(xi)* is the square of the standard uncertainty for the *xi* term.

Using Eq. (9.7), the combined standard uncertainty u_{N_ATC} in Eq. (9.6) is written:

$$u_{N\_ATC} = N^{ATC}\sqrt{\left(\frac{u_{Weibull}}{Weibull}\right)^2 + \left(\frac{u_{AF}}{AF}\right)^2 + \left(\frac{u_{N\_50}}{N_{50}}\right)^2} \tag{9.8}$$

where the sources of standard uncertainty for $u_{Weibull}$ and u_{AF} also have components of standard uncertainty and were derived using the first-order Taylor series as shown in Eq. (9.7). The estimated standard uncertainty $u_{Weibull}$ for the *Weibull* factor is

$$u_{Weibull} = \sqrt{\frac{\ln\left(\left(\frac{\ln(1-F\%\times 0.01)}{\ln(0.5)}\right)^2\right)}{\gamma^4}u_\gamma^2} \tag{9.9}$$

where: $F\%$ is the percent failed, γ is the shape parameter, and $u\gamma$ is the estimated uncertainty of shape factor γ.

The estimated standard uncertainty u_{AF} for the *AF* factor of Eq. (2.2) is

$$u_{AF} = \sqrt{\left(\ln\left(\frac{\Delta T^{DOS}}{\Delta T^{ATC}}\right)\right)^2 u_{\Delta T}^2 + \left(\ln\left(\frac{f^{ATC}}{f^{DOS}}\right)\right)^2 u_f^2 + \left(\frac{1}{T^{ATC}} - \frac{1}{T^{DOS}}\right)^2 u_e^2} \tag{9.10}$$

where: $u_{\Delta T}$ is the estimated uncertainty in the ΔT exponent of 1.9 found in Eq. (2.2), u_f is the estimated uncertainty in the f exponent of 1/3 found in Eq. (2.2), and u_e is the estimated uncertainty in the exponential constant 1414 found in Eq. (2.2).

The sample standard deviation of Eq. (9.2) serves as the estimated standard uncertainty $u_{N\_50.}$ The total estimated standard uncertainty u_{N_50} for Eq. (9.2) is.

$$u_{N\_50} = \sqrt{\frac{SSE}{n_{sample} - 2}} \tag{9.11}$$

where: n_{sample} is the number of samples in the population and is equal to 7 for this study, and *SSE* is the error sum of squares of Eq. (9.2)and is equal to 54326. Using the values of 7 for n_{sample} and 54326 for *SSE* leads to an estimated standard uncertainty u_{N_50} of 105 cycles for this study.

Standard uncertainties may be grouped into two categories depending upon the method used to estimate their values: Type A standard uncertainties are derived using statistical methods; and Type B standard uncertainties are derived using other methods and scientific judgment [147]. For Type A uncertainties the standard uncertainty is the sample standard deviation, and for Type B uncertainties the standard uncertainty can serve as an estimate of the standard deviation [147]. For example, the standard uncertainty for u_{N_50} is of Type A because the sample standard deviation of N_{50} was used as the estimate of the standard uncertainty. However, the standard uncertainties *uWeibull* and u_{AF} are of Type B because there is no statistical data to derive a sample standard deviation for the constants in the *Weibull* factor of Eq. (9.4) and *AF* factor of Eq. (2.2). Rather, scientific judgment and experience were used to estimate a sample standard deviation for each of the constants in the *Weibull* factor of Eq. (9.4) and *AF* factor of Eq.

(2.2). Table 9-4 lists the values for both Type A and Type B components of the standard uncertainties.

Table 9-4. Values of Type A and B standard uncertainties.

Combined Standard uncertainty	Components of combined standard uncertainty	Type	Estimated Value
$u_{Weibull.}$ See Eq.(9.9)	u_γ: estimated standard uncertainty in the shape factor γ.	B	u_γ=1.0
u_{AF} See Eq. (9.10)	$u_{\Delta T}$: estimated standard uncertainty in the ΔT exponent of 1.9.	B	$u_{\Delta T}$ =0.2
	u_f : estimated standard uncertainty in the f exponent of 1/3.	B	u_f =0.2
	u_e estimated standard uncertainty in the exponential constant of 1414.	B	u_e=500
u_{N_50} See Eq. (9.11)	--	A	u_{N_50} = 105

Often times a conservative estimate of the 95% confidence intervals is all that is desired for uncertainty in the fatigue life prediction. In this case, an approximation of the expanded uncertainty in (9.6 with a coverage factor k of 2 can be approximated by using ±25% of $NATC$ as the confidence interval (CI). In other words, 95% of the fatigue lives will fall within the range of $N^{ATC} \pm 0.25 \times N^{ATC}$. It will be seen in section 9.4 that this assumption is valid. However, insight into which factors contribute the most to uncertainty is lost when using the simplification ±0.25 x $NATC$ for the 95% confidence intervals.

9.2.6. Universal Fatigue Life Prediction Equation for CBGA Electronic Packages under Thermal Cycling

The final universal fatigue life prediction equation for CBGA is arrived at by expanding Eq. (9.6) as shown in Eq. (9.12).

Universal CBGA Predictive Equation for Thermal Cycling

$$N^{ATC} = (Weibull \pm u_{weibull}) \times (AF \pm u_{AF}) \times (N50 \pm u_{N50}) = \left(\frac{\ln(1 - F\% \times .01)}{\ln 0.5}\right)^{\frac{1}{\gamma}} \times \left(\frac{135}{\Delta T^{ATC}}\right)^{1.9} \left(\frac{f^{ATC}}{2}\right)^{1/3} \left(e^{1414\left(\frac{1}{T_{peak}^{ATC}} - \frac{1}{383}\right)}\right) \times \left[12476 - 0.241A - 719.9B - 1728C - 1381D - 12456E + 78.7BC + 72.4BD + 220CD\right] \quad (9.12)$$

A	Substrate Size (mm). 25-32.5mm	ΔT	Temperature Range, Kelvin
B	CTE Mismatch. 7.4-11.2 ppm/°C	f	Frequency, cycles per hour
C	Substrate Thickness. 0.8-2.9mm	T_{peak}	Peak Temperature, Kelvin
D	PWB Thickness. 1.57-2.8mm	$F\%$	Failure Percentage. $0 < F\% < 100\%$
E	Pitch. 1.00mm-1.27mm	γ	Shape Parameter, 4-11 for
		$u_{weibull}$	Estimated uncertainty of the *Weibull* factor. See Eq. (9.9)
$u_{N\_ATC} = N^{ATC}\sqrt{\left(\frac{u_{Weibull}}{Weibull}\right)^2 + \left(\frac{u_{AF}}{AF}\right)^2 + \left(\frac{u_{N\_50}}{N_{50}}\right)^2}$		u_{AF}	Estimated uncertainty of the AF factor. See Eq. (9.10)
See Eq. (9.8)		u_{N_50}	Estimated uncertainty of N_{50} regression equation. See Eq. (9.11)

9.3. DISCUSSION OF THE PREDICTOR VARIABLES

Now that a universal equation has been developed, it can be used to study the effect of several parameters on solder joint fatigue life.

9.3.1. Substrate Size and Number of Solder Joints

If one were to be given any two of the parameters such as the substrate size (A), the solder joint pitch (E), and the number of solder joints (n_{joints}), the third parameter can be estimated as approximately

$$n_{joints} = \left(\frac{A}{E}\right)^2 \quad (9.13)$$

In deriving the above equation, it is assumed that substrate is square in shape and also that there is a full square array of solder joints with the outermost rows of solder joints

being half a pitch away form the edge of the substrate. Table 9-5 shows the representative number of solder joints for different substrate size and different solder pitch. The numbers presented in Table 9-5 are different from the estimates from Eq. (9.13), as some of the solder joints are removed in commercially available CBGA packages for reliability, assembly, and other reasons.

Thus, if one were to keep the number of solder joints constant, one can show that the fatigue life decreases by 31% from 1543 cycles to 1071 cycles when the substrate size *(A)* is increased from 25 mm to 32.5 mm and the pitch increases from 1.27mm to 1.65mm, as illustrated in Table 9-5for Case 1 and Case 2. This decrease in fatigue life is expected due to the increase in the distance from the neutral point (DNP) of the outermost solder joint as the substrate size (A) increases. However, if one were to keep the pitch to be the same, the number of joints will increase with the increase in substrate size *(A)*, and thus, there is negligible change in the fatigue life of the outermost solder joint as seen in Case 1 and Case 3 of Table 9-5. This is because the increase in n_{joints} keeps the load per solder joint approximately the same and thus helps to offset the larger DNP effect. The predictions shown in Table 9-5 use a CTE mismatch *(B)* of 11.2 ppm/^{o}C, a substrate thickness *(C)* of 0.8mm, a PWB thickness *(D)* of 1.57mm, and an ATC of 0/100^{o}C 3cph.

Table 9-5. Comparison of Substrate Size and Number of Solder Joints

Case	Substrate Size *A* (mm)	n_{joints}	Pitch *E* (mm)	N^{ATC}
1	25x 25	388	1.27	1543
2	32.5 x 32.5	388	1.65	1071
3	32.5 x 32.5	656	1.27	1545

However, in actual industrial practice, the larger DNP reduces the fatigue life of the outermost solder ball [126, 148], and this decrease may be due to several factors: 1) Several larger packages do not have a fully populated area array of solder joints. Rather, they have selected interior rows depopulated for various reasons, and therefore, the load

taken by each solder ball along a given row will increase, and thus the fatigue life will decrease; 2) Several assembly/process-induced issues such as planarity of large substrate/board, solder ball alignment, stand-off height variations, etc. will also affect the reliability, especially when the package is larger. Such variations are difficult to address in the finite-element model, and therefore, included as process variations under section 3.5; 3) Eq. (9.12) shows that the fatigue life will decrease with the substrate size as indicated by the negative coefficient for the substrate size parameter (A). However, the magnitude of this negative coefficient (-0.241) is not high enough to significantly influence the fatigue life. This indicates a weakness in the FEM regarding the substrate size effect only. Further modeling work along with experimental tests where substrate size is the only variable to change could be done to determine a better correlation.

9.3.2. CTE mismatch between the substrate and board

When different substrate materials are used in CBGAs, the CTE mismatch (*B*) between the substrate and the board will change. Table 9-6 shows the properties of two materials commonly used for CBGA substrates.

Table 9-6. Material Properties for Ceramic Substrate

Material	Temp (K)	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm/K)
Alumina Al_2O_3	298	241	0.25	6.8
High CTE Glass	298	74	0.25	10.6*

*Measured by [149]. Manufacturer lists as 12.3 ppm/K [117]

It can be observed in Table 9-6 that when substrate material is different, the CTE and the modulus are also different. The change in substrate modulus is assumed to have a second order effect on the solder joint fatigue life within the class of ceramics [125], and therefore, is not considered in the development of the universal predictive equation.

9.3.3. Pitch and Solder Joint Geometry

When the solder joint pitch is changed, the solder joint diameter, the standoff height, the pad size on the substrate and the board side, and the solder paste volume will proportionately change. Therefore, whenever the pitch is changed, the corresponding solder geometry, pad size, and solder volume are changed during the development of the regression equation presented in this paper. Such proportional changes in solder geometry, pad diameter, and solder volume can be found in the open literature. For example, several studies have been performed to determine the optimum paste volumes and pad diameters [13, 140, 150-152]. The values used in this work are those given by IBM [126] as shown in Table 9-7.

Table 9-7. Proportional Changes in CBGA Solder Balls, Pads, and Solder Paste Volume with Solder Joint Pitch [126].

Pitch (mm)	Solder joint diameter (mm)	Board pad diameter (mm)	Substrate pad diameter (mm)	Solder paste volume on board side (mm^3)
1.27	0.89	0.72	0.86	0.10 - 0.12
1.00	0.80	0.68	0.80	0.05 - 0.07

Therefore, although parameters such as solder joint diameter, solder joint standoff height, pad diameters, and solder paste volume are not explicitly included in the universal predictive equation, they are implicitly accounted for when the solder joint pitch is changed.

9.3.4. Substrate and Board Thickness

As the board and/or the substrate thickness is increased, the solder fatigue crack location shifts from the substrate side to the board side of the solder joint, and also, the fatigue life, in general, decreases. This has been observed experimentally [153]. The same phenomenon is also seen in the finite-element models where the total strain energy density at the board side increases as the board thickness and/or the substrate thickness is

increased. It is worth noting that this interaction between the substrate thickness and the board thickness is captured in the predictive equation. Increasing the board thickness has more adverse effect on the fatigue life for a CBGA with a thin substrate than a CBGA with a thick substrate [127].

9.3.5. Other Considerations

Beyond the several parameters that are discussed above, the solder joint fatigue life is dependent on other parameters that are not discussed in this paper. For example, for thermal management purposes, heat-sink lids are often attached to the CBGA package. Two types of such lids are possible; a standard lid that is attached to the substrate and a direct lid attach (DLA) that is attached to the backside of the die and is primarily for thermal purposes. The lid has the following effects on the solder joint fatigue life: 1) The presence of a lid acts to stiffen the ceramic substrate [126, 154], and therefore, will reduce the solder joint fatigue life and 2) The additional weight of the lid reduces the solder joint standoff height under high temperatures [149], and thus, will reduce the solder joint fatigue life. A standard aluminum lid attach reduces the fatigue life by anywhere from 5-40% depending upon the compliancy of the lid attach material [149, 154], the substrate thickness [127], and the CTE mismatch between the lid and ceramic substrate [149, 154]. The lid effect is less for thicker substrates which already have increased stiffness [127]. The presence of an aluminum DLA reduces the fatigue life by approximately 20% [126].

In addition to the attached lid, there are other factors that affect the solder joint fatigue life. When the temperature extremes become harsh, solder joint fatigue failure near the board side is commonly observed [148]. In several CBGA packages, the six corner solder joints are often depopulated for shipping and handling reasons. This depopulation of corner joints, especially for 1 mm pitch CBGAs, has been accounted for in the developed models.

Underfill may also be used for CBGAs in order to enhance solder joint reliability [145]. When underfill is used, the coefficients and the parameters in the universal fatigue-life equation will also change. Accordingly, a new universal fatigue-life equation has to be developed for CBGAs with underfill. However, the methodology proposed in this work will still remain the same for CBGAs with underfill, and also for PBGAs with underfill and/or conformal coating.

Additionally, process and manufacturing variations such as planarity of large substrate/board, solder ball alignment, stand-off height variations, solder paste volume, variation in material quality, etc. will play a role in the reliability of solder joint fatigue life.

9.4. VERIFICATION OF PREDICTIVE EQUATION USING LITERATURE DATA

As a verification of the universal predictive fatigue equation, five sets of experimental data are taken from literature and the solder joint fatigue life predicted by the universal predictive equation is compared against the experimental data. The material data, geometry information, and loading conditions were taken from the literature and were used in the universal predictive model. Table 9-8 compares the predicted fatigue life (N_{50pred}) against experimental fatigue life (N_{50exp}). The second to last column of Table 9-8 uses equation (9.6) with a coverage factor k of 2 to obtain the 95% confidence intervals. As seen from Table 9-8, the experimental data falls within the predicted range in all of the cases. It can also be seen in the last column of Table 9-8 that using 0.25 x N_{50pred} in place of Eq. (9.6) serves as an approximate estimate of the 95% confidence intervals.

Table 9-8. Literature cases used to assess validity of the developed predictive equation

Case [reference]	Substrate Size (mm)	Substrate Thickness (mm)	Board Thickness (mm)	Pitch	Substrate Material	ATC	N_{50exp}	$N_{50pred} \pm 2u_{N\_ATC}$ (95% CI)	$N_{50pred} \pm (0.25 \times N_{50pred})$
8 [126]	25x25	0.8	1.57	1.27	Al_2O_3 Ceramic	0/100 3cph	3700	3449±574	3449±862
9 [155]	25x25	0.8	1.57	1.27	Al_2O_3 Ceramic	-55/110 2cph	1270	1054±190	1054±263
10[127]	32.5x32.5	1.0	1.83	1.27	Al_2O_3 Ceramic	0/100 3cph	2700	3026±551	3026±757
11[126]	32.5x32.5	2.4	1.83	1.00	Al_2O_3 Ceramic	-55/110 2cph	719	731±167	731±183
12[156]	32.5x32.5	2.9	1.57	1.27	Al_2O_3 Ceramic	-55/125 1cph	189	197±180	197±45

Although the case studies have shown the validity and the usefulness of the universal predictive equation, the following items should be kept in perspective before using the equation: (1) the universal predictive equation should be used only for the cases where the geometry, material, and loading conditions fall within the range that was used for developing the equation. Cases may arise where several of the predictor values fall within the range, while one or two may fall outside. Under those situations, suitable judgment should be exercised before applying the universal predictive equation. (2) the developed universal equation is based on two-level factorial analysis, and therefore, the equation is linear in nature. Such a linear relationship is appropriate for short ranges in the predictor variables. However, for larger ranges, three-level factorial analysis may be needed, as discussed in the following section. (3) Several other parameters are not considered in the development of the universal predictive equation, as these parameters usually do not have significant effect on the predicted fatigue life. (4) The developed universal predictive equation is applicable for lead-tin CBGA package family and should not be used for other package families.

9.5. APPLICATION: MILITARY OBSOLESCENCE AND MAINTANENCE SCHEDULING

Ball grid array (BGA) microelectronic packages are being increasingly used in the air force avionics. Several of these BGA packages are initially designed for commercial applications for mostly benign operating conditions with a life expectancy ranging from five to seven years. However, when they are used in military applications, several questions arise:

- Will the BGAs be reliable for military applications? Existing knowledge with the BGAs for military applications is very limited.
- How long will the BGAs last for military applications?
- How often should they be replaced? And when they are replaced, will the part be obsolete?

The developed universal polynomial predictive equation will be implemented into a spreadsheet tool allowing exploration of the questions above for several scenarios.

9.5.1. Condition-Based Maintenance. Example A

The proposed methodology is used to develop a tool for condition-based maintenance of avionics hardware. Depending on how long a component has been in use, the tool can recommend when to replace a particular component depending on the past and the proposed future usage conditions. Flight environments can be developed based on ambient temperature, peak temperature, and flight length. One can develop a HIGH usage condition and a LOW yearly usage condition as shown in Figure 9-2. HIGH usage averages out to 2 flights per day, and LOW usage averages out to 0.5 flights per day.

The spreadsheet tool will be illustrated using Motorola's PowerPC755 RISC microprocessor commonly used component in avionics hardware (Atmel, Radstone, SBS Technologies). The common parameters of the Atmel Power PC755 are, substrate size of 25mm, substrate thickness of 1.1mm, pitch of 1.27mm, and a CTE mismatch of 5.7 ppm/°C.

Figure 9-2 illustrates the tool in a questionnaire based form. Expected user inputs are in blue font.

Enter today's year (or a future year):	2007
What year was the component put in service?	2000
How many years between 2000-2007 were under HIGH (see table below) usage conditions?	1
Years of LOW (see table below) usage conditions:	6
Should the component be replaced now, based on N(1.00%) ?	No, replace the component in 1.6 years (2009), assuming LOW usage conditions.
Optional Items	
Failure based on N%:	1
Slope Paramater (β) for Wiebull Analysis.	6
Replacement Criteria (1.0 = total failure)	0.8

HIGH and LOW Yearly Usage Conditions

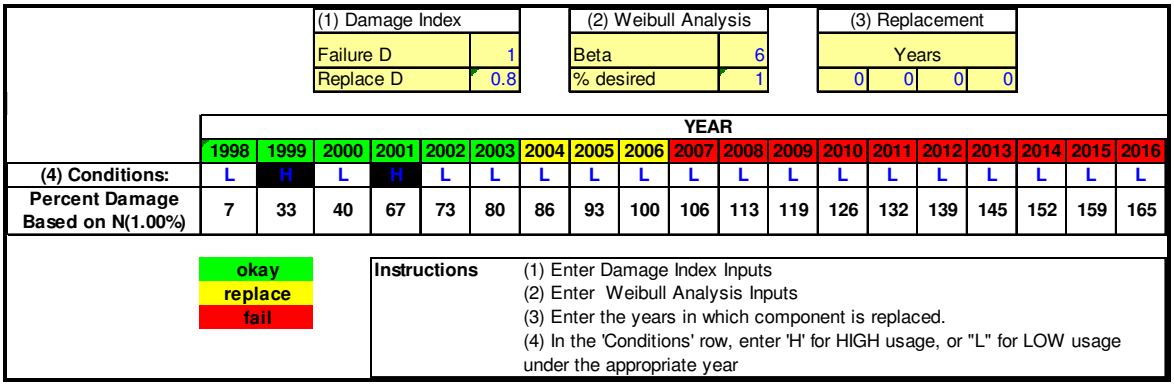
Flights Per Year		Operating Conditions		
HIGH Usage	LOW Usage	Ambient Temp, Celsius	Operating Temp, Celsius	Flight Length, Hours
3	0	-55.0	85	4
7	1	-42.5	85	4
18	4	-32.5	85	4
18	4	-22.5	85	4
22	5	-12.5	85	4
116	30	-2.5	85	4
207	53	7.5	85	4
220	56	17.5	85	4
116	30	27.5	85	4
2	0	37.5	85	4
2	0	49.0	85	4
731 flights per year.	183 flights per year.			
2.0 flights per day.	**0.5 flights per day.**			

Figure 9-2. Simple Analysis Tool for Avionics Maintenance. Example A

9.5.2. Condition-Based Maintenance: Example B

More complex, scenario-based decision making can be made by using an interactive table as shown in Figure 9-3. Using Figure 9-3, the years in which the component should be replaced, and when failure will occur can be determined. Each year can be adjusted to be a HIGH usage year or a LOW usage year. Figure 9-3 illustrates the tool given 2 HIGH

usage years in 1999 and 2001. Fatigue life based on N(1%) will be used to make replacement decisions.



(1) Damage Index		(2) Weibull Analysis		(3) Replacement			
Failure D	1	Beta	6	Years			
Replace D	0.8	% desired	1	0	0	0	0

	YEAR																		
	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016
(4) Conditions:	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Percent Damage Based on N(1.00%)	7	33	40	67	73	80	86	93	100	106	113	119	126	132	139	145	152	159	165

okay
replace
fail

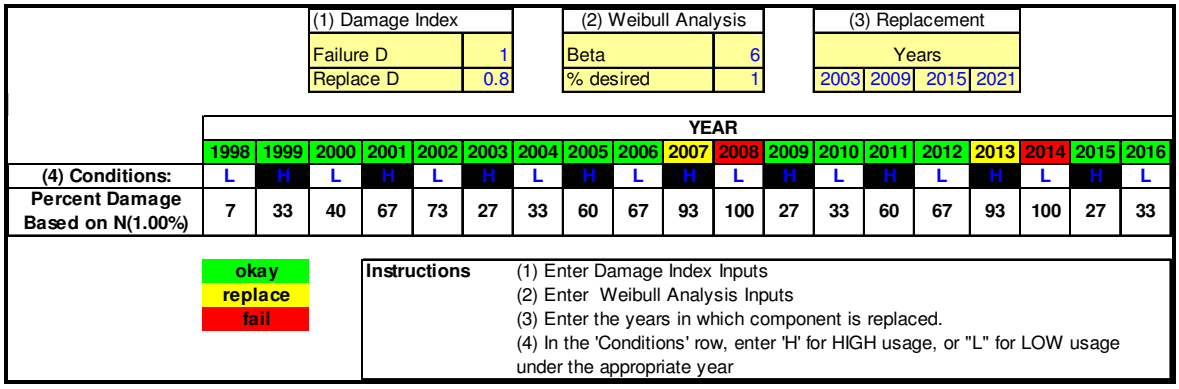
Instructions
(1) Enter Damage Index Inputs
(2) Enter Weibull Analysis Inputs
(3) Enter the years in which component is replaced.
(4) In the 'Conditions' row, enter 'H' for HIGH usage, or "L" for LOW usage under the appropriate year

Figure 9-3. Complex Analysis Tool for Avionics Maintenance. Example B

From Figure 9-3 it can be seen that the component should be replaced in 2004, or in 2006 at the latest. By typing in 2006 into area (3) in Figure 9-3, the reader can see the effect of replacing the component in the year 2006.

9.5.3. Periodic Maintenance: Example C

Figure 9-4 shows a scenario where there is a periodic replacement every 6 years, and where there are alternating HIGH usage years.



(1) Damage Index		(2) Weibull Analysis		(3) Replacement			
Failure D	1	Beta	6	Years			
Replace D	0.8	% desired	1	2003	2009	2015	2021

	YEAR																		
	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016
(4) Conditions:	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
Percent Damage Based on N(1.00%)	7	33	40	67	73	27	33	60	67	93	100	27	33	60	67	93	100	27	33

okay
replace
fail

Instructions
(1) Enter Damage Index Inputs
(2) Enter Weibull Analysis Inputs
(3) Enter the years in which component is replaced.
(4) In the 'Conditions' row, enter 'H' for HIGH usage, or "L" for LOW usage under the appropriate year

Figure 9-4. Periodic maintenance tool: Example C

From Figure 9-4 it can be seen that the 6-year periodic maintenance schedule is not adequate based on N(1%). One out of 100 components is likely to fail in the years 2007

and 2013. The reader is encouraged to experiment with the replacement years in area (3) until an adequate solution is found.

9.6. CONCLUSIONS

An innovative methodology to predicting solder joint fatigue life that combines the strength of mechanics-based finite-element formulation, sets of experimental data, and design of simulations has been developed. Using the developed methodology, a universal predictive universal fatigue life equation for CBGA electronic packages has been formulated. The universal equation accounts for CBGA geometry/material parameters such as the substrate size, CTE mismatch between the substrate and board, substrate thickness, board thickness, and solder joint pitch. The model is easy to use, time-effective, and does not require advanced mechanics and finite-element knowledge, and thus can be used by any designer in the early stages of design. The model has been validated with various other experimental data that were not used in the development of the universal equation. The model has been extended to include uncertainty terms due to failure distribution, acceleration parameters, and regression modeling. The model can be extended to include additional parameters such as presence of a lid, the presence of a heat sink, the use of underfill, etc. For those cases where the number of predictors increases, fractional factorial designs may be necessary. The developed methodology can be extended to PBGA, Pb-free CBGA, and other packages.

The advantage of the developed methodology is illustrated in the ease in which it can be implemented into a spreadsheet tool designed for establishing a periodic maintainence program for CBGA components in avionics hardware.

Additionaly, to make the universal predictive equation more intuitive in terms of which parameters play the greatest role, the design parameters could have been normalized, say to values between 0 and 1, so that the sign and magnitude of the coeffecient would be an

indication of how greatly the design parameter increases or decreases the magnitude of the fatigue life.

CHAPTER 10

ACCELERATION FACTOR TO RELATE THERMAL CYCLES TO POWER CYCLES FOR CERAMIC BALL GRID AREA ARRAY PACKAGES

10.1. INTRODUCTION

Using the methodology outlined in chapter 9, this chapter develops universal predictive polynomial fatigue equations for ATC and PC for CBGA packages. Once such equation are developed, this chapter derives an acceleration factor (AF) relationship between ATC and PC. This relastionship takes into account the differences between ATC tests and PC tests for ceramic ball grid array (CBGA) packages by considering relevant design and environmental parameters.

The ATC and PC universal predictive equations, and the acceleration factor equation, are based on design parameters such as substrate thermal conductivity, substrate thickness, coefficient of thermal (*CTE*) mismatch between the substrate and printed wiring board (PWB), PWB thickness, and environmental parameters such as temperature range (ΔT), frequency of cycles (f), and peak/junction temperature (T_j). The new AF can be used to more accurately assess PC fatigue life from ATC tests so that expensive over-designing of electronic packages can be avoided.

10.2. POWER CYCLING THERMAL ENVIRONMENT

A brief background into power cycling is given in order to understand how heat is removed from the chip, and understand why thermal gradients develop in the electronic package. The thermal performance of electronic packages is commonly measured by the use of the one-dimensional die junction-to-ambient thermal resistance Θ_{ja}:

$$\theta_{ja} = (T_j - T_a)/Q_{Die} \tag{10.1}$$

where T_j is the junction (peak) temperature of the die , T_a is the ambient temperature and Q_{Die} is the power applied to the die. The thermal network shown in Figure 10-1 can be used to estimate Θ_{ja} and analyze the thermal requirements and/or limitations [22, 157, 158]. As seen in Figure 10-1, the heat Q from the die flows through the heatsink as well as through the solderball/PWB. The heat is then dissipated to the ambient air through convection. Radiation effects are neglected due to junction temperatures of less than 100°C encountered in the forced airflow environment.

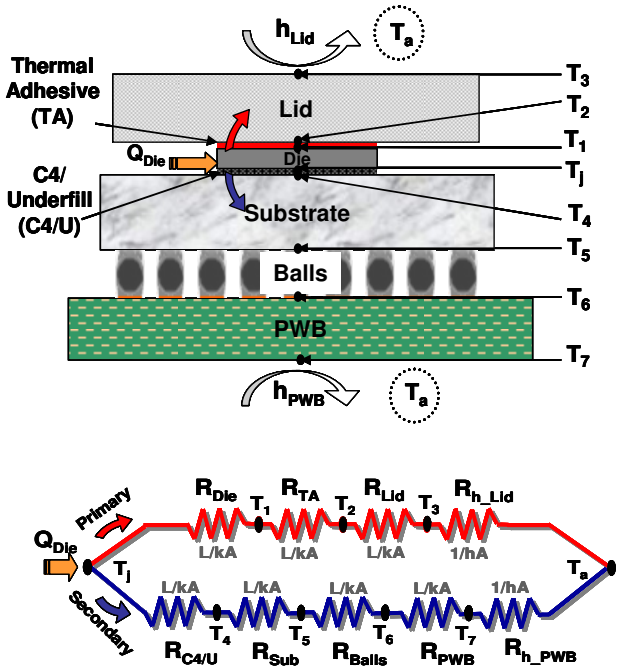


Figure 10-1. 1D Thermal Resistor Network for CBGA

The thermal network in Figure 10-1 enables a simplistic understanding of the heat paths, however, it is one-dimensional and does not account for 3D heat flow which results in temperature gradients across the package and heat loss from the sides. As the one-dimensional resistor-network model does not account for 3D heat flow, a 3D quarter-symmetry finite element model is developed to more accurately determine the temperature distribution and to determine solder joint fatigue thermo-mechanical fatigue life.

10.3. CERAMIC BALL GRID ARRAY (CBGA)

A 25x25mm CBGA with 361 solder balls on a 1.27mm pitch assembled to an FR4 board is used to illustrate the method for developing an AF to relate ATC to PC tests. As a first step in developing the AF, finite-element models are developed to determine the temperature contours and solder joint strains. The following sections discuss the features of the CBGA packaging assembly as well as the modeling details and assumptions:

- A high conductivity 1S2P FR4 board with 1% copper content by volume in the vertical for vias in the board is assumed. The board size is 114x101 mm (4"x4.5") according to JEDEC standards. Typical JEDEC standards use a low conductivity board, however this study is considering a board with vias likely to be used in a real application. Using FEM and composite rule of mixtures, preliminary studies show that including 1% by volume of copper as vias in the thickness of the board raises the thermal conductivity from 0.26 W/m °C to 3.9W/m °C. Above 2% copper, or a thermal conductivity of 7.5 W/m °C there is little change in the temperature distribution, warpage of the board, and fatigue life. This is consistent with findings from other researchers [32]. Table 10-1 lists the preliminary study.

Table 10-1 Effect of PWB normal thermal conductivity

% Cu in normal direction	k_{normal} PWB (W/m °C)	ΔT in PWB normal (°C)	Normalized N_{50}
0%	0.26	11.2	1
1%	3.85	2.1	0.92
2%	7.45	1.4	0.91

- This study considered a board with 1% by volume of copper in the normal direction to represent vias likely to be used in a real application.
- The 2nd level interconnect BGA balls consist of a 90Pb10Sn 0.89 mm diameter ball with 63Sn37Pb solder paste. The 90Pb10Sn has a higher melting point than the 63Sn37Pb solder paste and therefore, does not melt during reflow. Thus, a constant standoff height can be achieved during reflow. Solder paste volume on the board side is 0.091 mm^3 and above the minimum of 0.089 mm^3 suggested by IBM [126]. 0.72mm diameter copper pads are used on the board side, and 0.68mm diameter molybdenum pads are used on the substrate side. Other relevant modeling parameters can be seen in [142, 143].
- A 12.7x12.7x0.738 mm silicon die is attached to the top of the substrate using a C4 flip chip interconnection with an epoxy underfill.

- A 23x23x2 mm aluminum lid is attached directly to the back of the die with a thermal adhesive having a 0.1 mm bondline. The direct lid attach (DLA) is used as a heat spreader for the next level of thermal management.
- A power density of 25 W/cm^2 (40W for a 12.7x12.7 mm die) is used. This power density is typical of an ASIC design.

10.4. METHOD TO DEVELOP ACCELERATION FACTOR FOR RELATING ATC TO PC

The methodology of Table 9-1 will now be used to develop universal polynomial predictive fatigue life equations for a CBGA under ATC and PC environments. The universal polynomial predictive developed in chapter 9 for ATC could be used in this chapter for the ATC portion. However, since the boundary conditions and geometry of this chapter necessitate including a lid there is reasonable justification as indicated in section 9.3.5 to develop another polynomial predictive fatigue equation for ATC that includes the effect of a lid. Additionally, a universal polynomial predictive equation for a CBGA in a PC environment is developed. The developed equations will then be used to derive an AF to relate ATC to PC by taking the ratio of N_{PC}/N_{ATC}..

The details of the Finite Element Model (FEM), material properties, developing the fatigue life prediction equation, and forming the ATC and PC predictive design based equations are now described.

10.4.1. Steps 1-3: Development of Coffin-Manson type equation for fatigue life prediction

According to Table 9-1. Steps to derive the universal predictive fatigue life equationThe first three steps have been covered in previous chapters. Chapter 5 discussed the development of a unified finite-element model, and Chapters 6 and 7 discussed the development of fatigue-life prediction equation and the validation of the finite-element model. The total strain based equation (7.2) is used to predict the mean fatigue life N_{50} using the unified FEM. The following sections discuss the remaining steps in the development of the universal polynomial predictive equation.

10.4.2. Steps 4 and 5: Design of Simulations (DOS)

After determining the Coffin-Manson coefficients using experimental data and finite-element analysis as discussed above, the finite-element models are used to perform parametric analysis to understand the effect of various parameters under accelerated thermal cycling as well as power cycling. The design parameters chosen for the ATC environment are: substrate thickness (*A*) ranging from 0.8 to 2.9 mm, PWB thickness (*B*) ranging from 1.57 to 2.8 mm, and CTE mismatch (*C*) ranging from 7.4 to 11.2 ppm/°C. Pitch is neglected because previous studies [142] concluded the pitch had a secondary effect for ATC cycling on CBGA electronic packages. Also, the substrate size is held constant as 25 mm square. The design parameters chosen for the PC environment are the same as the ATC environment with the addition of the substrate conductivity (*D*) ranging from 0.002 to 0.021 W/mm °C. The substrate conductivities of alumina ceramic and a high CTE glass ceramic are an order of magnitude different, and thus the temperature gradient in the substrate, ΔT_{sub}, and the solder fatigue life will also be different for different substrate material.

Both ATC and PC simulations were started with a stress-free solder melting temperature of 183°C and cooled down to a room temperature of 25°C. For ATC, the assembly was cycled between 0 to 100°C at 3 cph with 5-minute ramps and 5-minute dwells resulting in ramp-up and ramp-down rate of 20 °C/minute. For PC, the assembly was cycled between room temperature (30°C) and a junction temperature of 100°C by using a 40W die and with an appropriate convection coefficient to ensure that the junction temperature is 100°C. In real life applications it not desirable to have the junction temperature exceed 80°C. The high temperature of 100°C used in the PC simulations is to account for temperatures that may exceed 80°C nominally, and to overlap the ATC thermal conditions. For PC simulations, a transient thermal analysis was done prior to the thermo-mechanical structural analysis. When the die is powered, it is seen that the ramp up temperature rate is 30°C/minute, and when the die is switched off, it is seen that the

ramp down rate is 30^0C/minute. As the ramp durations were shorter for PC compared to ATC (due to faster ramp rate and smaller temperature range), the PC dwell times were longer to ensure the same cyclic frequency between ATC and PC as seen in Figure 5.

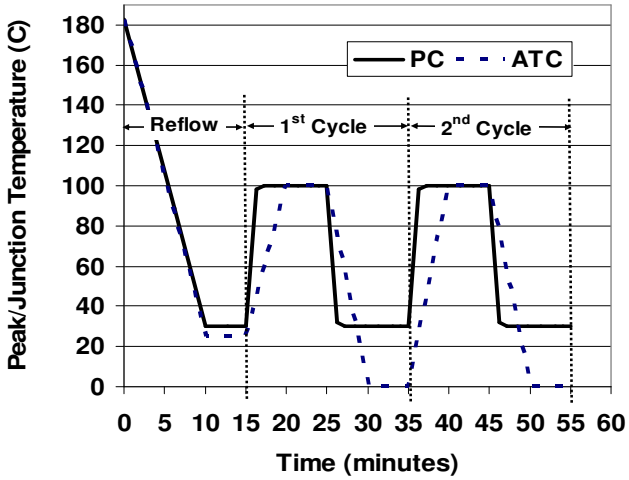


Figure 5. ATC and PC simulated cycles for Design of Simulations (DOS).

An important difference between ATC and PC is the absence of temperature gradients in ATC and the presence of temperature gradients in PC. Therefore, in addition to keeping the maximum temperature, the number of cycles per hour, stress-free temperature, and other geometry parameters identical between ATC and PC, it is also essential to understand how the thermal gradients would affect solder reliability. The h_{eff} and Q_{die} applied may affect the temperature distribution in the rest of the package and therefore the solder joint fatigue life. To assess whether this was possible, two cases were run at die powers of 10W and 100W. Appropriate h_{eff} was applied to get T_j= 100^0C for both power levels. It was determined that the temperature distribution in the package is relatively independent of the h_{eff} and Q_{die}, given that the junction temperature T_j is fixed. In other words, it is the T_j that determines solder joint fatigue life and not the cooling solution on the die or power applied in the die.

The finite-element models with the load profiles discussed thus far were used to perform design of simulations for ATC and PC. For the three parameters identified for ATC

(substrate thickness (*A*), PWB thickness (*B*), and CTE mismatch (*C)*) at two levels for each parameter, a full factorial analysis consisting of eight runs was carried out. Similarly, for PC four parameters (substrate thickness (*A*), PWB thickness (*B*), CTE mismatch (*C)*, and substrate thermal conductivity *(D)*) at two levels for each parameter, a full factorial analysis consisting of 16 runs was carried out. For each run, the volume averaged inelastic accumulated strain per cycle was determined using the FEM simulation, and the solder fatigue life was computed using (3). For all of the cases simulated, it was seen that the outermost solder joint had the highest volume averaged inelastic accumulated strain per cycle, and therefore, the lowest fatigue life.

10.4.3. Step 6a: Analysis of Variance (ANOVA)

An ANOVA analysis will help determine the predictors that have a significant effect on the response. ANOVA analysis using MINITAB™ [159] was performed to determine important main effects and interaction effects. Using normal probability plots with a confidence interval of 95% the significant main effects in order of importance are substrate conductivity (*D)* and CTE mismatch *(C)* for PC. For ATC, CTE mismatch *(C)* and substrate thickness *(A)* are considered the most important main effects respectively. The interaction effect of the substrate thickness and PWB thickness (*AB)*, along with the interaction effect of the substrate thickness and CTE mismatch *(AC)* are considered important for ATC. For PC, numerous interaction effects including *AB, BC, AC, AD, ABC,* and *ACD* are considered important. These results are confirmed by observing the main effects and interaction plots (not shown). It is worth noting that the substrate conductivity does not affect the ATC fatigue life.

10.4.4. Step 6b: Regression Analysis

Now that we have determined the influential predictors on the response, we can develop linear regression equations that relate the responses to the predictors. A best subset regression for each environment was performed to determine the best regression model

using a criteria of R^2(adj), the C_p statistic, and the standard deviation (σ). The C_p value of the regression analysis indicates the optimum number of terms to be used in the regression analysis and should be equal to the number of predictors in the equation. For additional details on the development of regression equation, please refer to [142].

The ATC regression equation shown in Eq. (10.2) an R^2(adj) of 99.8%, a C_p statistic of 5.4, and a standard deviation of $\sigma = 73$. The PC regression equation shown in Eq. (10.3) and has an R^2(adj) of 96.9%, a C_p statistic of 4.17, and a standard deviation of $\sigma = 297$.

$$N_{50\_ATC} = 13905 - 1812\ A - 940\ B - 766\ C + 285\ A*B + 38.3\ A*C \tag{10.2}$$

$$N_{50\_PC} = 85011 - 4005\ C - 1688849\ D + 10949\ A*B + 452\ B*C + 493\ A*C - 1604171\ A*D - 1251\ A*B*C + 142010\ A*C*D \tag{10.3}$$

The ratio between Eq. (10.3) and Eq. (10.2) will give the AF between PC of 30/100°C 3cph and ATC of 0/100°C 3cph for a wide range of geometry parameters for a CBGA. However, such a ratio is limited in scope, as one would like to know the AF for other temperature ranges as well as other cycling frequencies. Furthermore, the derived equations are limited to N_{50} fatigue life. Therefore, in the next section, we will augment the above equations to include these other parameters.

10.4.5. Step 7: Norris-Landzberg AF and Weibull Analysis

The regression models developed so far in (10.2) and Eq. (10.3) are for accelerated thermal cycling for an ATC of 0/100°C 3cph and a PC of 30/100°C 3cph respectively. To determine the N_{50} fatigue cycles for other ATC and PC conditions, the Norris-Landzberg equation [7], (6), can be used to determine the AF as in section 9.2.4.

In addition to different ATC conditions, it is also important to be able to determine the fatigue life for 1%, 63.2% and other percentage failures. For example, finding the solder joint fatigue life at a probability other than 50% is of interest for applications requiring

high reliability such as medical and military applications where 1% fatigue failure is desired. A two-parameter Weibull analysis is used to predict the fatigue life at percentages other than the mean life at 50%, N_{50}, as described in section 9.2.4.

10.4.6. Step 8: Final Predictive Fatigue Life Equations and AF for relating ATC to PC

The final predictive equations are developed by expanding Eq. (9.5) for each environment as shown in Eq. (10.4) for ATC and Eq. (10.5) for PC as shown in Table 10-2.

Table 10-2. Final Fatigue Predictive Equations for ATC and PC

$N_{F\%}^{ATC} =$ $\left[\left(\frac{\ln(1.0-.01F\%)}{\ln 0.5}\right)^{\frac{1}{\beta}} \times \left(\left(\frac{100}{\Delta T^{ATC}}\right)^{1.9}\left(\frac{f^{ATC}}{3}\right)^{1/3} e^{1414\left(\frac{1}{T_{peak}^{ATC}}-\frac{1}{373}\right)}\right)\times \left(13905-1812A-940B-766C+285A*B+38.3A*C\right)\right]$	(10.4)
$N_{F\%}^{PC} =$ $\left[\left(\frac{\ln(1.0-.01F\%)}{\ln 0.5}\right)^{\frac{1}{\beta}} \times \left(\left(\frac{70}{\Delta T^{PC}}\right)^{1.9}\left(\frac{f^{PC}}{3}\right)^{1/3} e^{1414\left(\frac{1}{T_{peak}^{PC}}-\frac{1}{373}\right)}\right)\times \left[85011-4005C-1688849D+10949A*B+452B*C+493A*C-1604171A*D-1251A*B*C+142010A*C*D\right]\right]$	(10.5)

A	Substrate Thickness (0.8-2.9 mm)	ΔT	Temperature Range of cycle
B	PWB Thickness (1.57-2.8mm)	f	Frequency of cycles (cycles per hour)
C	CTE Mismatch (5.8-11.2 ppm/°C)	T_{peak}	Peak/Junction Temperature of cycle
D	Substrate Conductivity (0.002-0.021 W/mm °C)	$F\%$	Failure Percentage
		β	Shape Parameter, 4-12 for CBGA

The ratio of Eq. (10.5) and Eq. (10.4) given in Eq. (10.6) provides the AF to relate ATC fatigue life to PC fatigue life based on design parameters.

$$AF_{ATC}^{PC} = \frac{N_{F\%}^{PC}}{N_{F\%}^{ATC}} \tag{10.6}$$

10.5. APPLICATION OF DEVELOPED AF EQUATION

Several examples and conclusions will now be presented using the developed predictive equations and acceleration factor to relate ATC to PC. The four cases presented in Table 10-3 will be used in the following discussions. A shape parameter β of 11 is used for all Weibull distributions.

Table 10-3. Test Cases for AF relating PC to ATC

CASE	Substrate Thickness (mm)	PWB Thickness (mm)	CTE Mismatch (ppm/ °C)	Substrate Cond. (W/mm °C)
1	0.8	1.57	11.2	0.002
2	0.8	1.57	11.2	0.021
3	2.9	2.8	11.2	0.021
4	2.9	2.8	7.4	0.002

10.5.1. Effect of substrate thermal conductivity on PC fatigue life.

The effect of substrate CTE on solder joint fatigue life has been well studied, and it is known that under ATC and PC, lower CTE mismatch between the substrate and the PCB will increase the fatigue life of CBGA solder balls. However, the effect of the substrate thermal conductivity on CBGA fatigue life under PC has not been studied.

When the thermal conductivity is decreased from 0.021 W/mm °C (Case 2) to 0.002 W/mm °C (Case 1), the PC solder fatigue life shows a 3.0 times improvement, as seen in Table 10-4, for the same die power of 40W applied at a frequency of 0.25cph and convection cooling of 1365 W/mm^2 K on top of the aluminum lid.

Table 10-4 Comparison of high and low substrate thermal conductivity.

CASE	N_{50} PC	Increase in PC Fatigue life
1) 0.002 W/mm °C	23675	3.0x
2) 0.021 W/mm °C	7910	

For this example, switching to the lower thermal conductivity board resulted in a four degree Celsius increase in the die junction temperature ΔT_j but the temperature across the substrate was twenty-one degrees Celsius lower than in the higher thermal conductivity case as shown in Figure 10-2. This decrease in temperature across the substrate results in a higher fatigue life because less heat is removed through the substrate secondary path and thus the temperature of the substrate and PWB is lowered. The drawback to lowering the substrate conductivity is that a more efficient cooling solution on the primary path must be used.

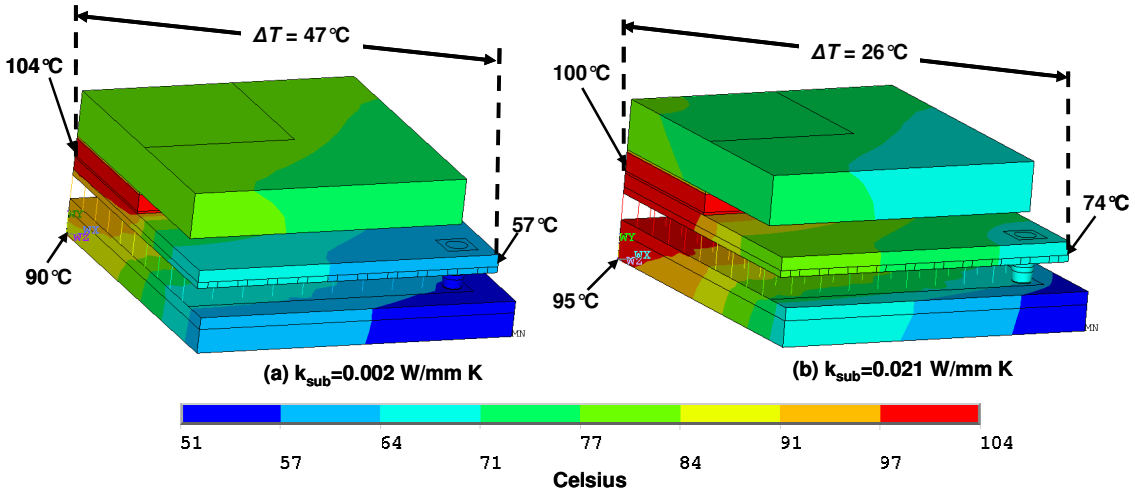


Figure 10-2. Temperature gradients for (a) Case 1, k_{sub} = 0.002 W/mm K, and (b) Case 2, k_{sub} = 0.021 W/mm K.

10.5.2. Benefits of HICTE glass ceramic substrates compared to alumina ceramic

If one were to use HICTE glass ceramic substrate instead of alumina ceramic, the solder ball fatigue life will increase under ATC as well as PC due to the lower CTE mismatch between the substrate and the PWB. Furthermore, due to the lower thermal conductivity of HICTE glass ceramic substrate compared to alumina ceramic, the solder joint fatigue life will further increase fatigue life in PC due to the reasons discussed in the previous section. The last row in Table 10-5 shows the improvement in fatigue life for both ATC and PC for HICTE compared to alumina ceramic. Also, the last column in Table 10-5 shows the acceleration factor between ATC and PC, and it is clear that without the

methodology developed in this work, the acceleration factor will be underestimated and the package design may be over conservative.

Table 10-5. Alumina and HICTE substrate comparison

CASE	N_{50} ATC	N_{50} PC	AF for ATC to PC
3) Alumina	1590	7431	4.7x
4) HICTE	5557	58419	10.5x
Increase in N_{50}	3.5x	7.8x	

It should be noted that performing ATC tests would not have captured the added benefit of a lower substrate thermal conductivity on solder joint fatigue reliability.

10.5.3. Estimating the number of ATC cycles to qualify a product based on required PC field life

ATC tests are often preferred over PC tests due to the simplicity and lower cost of ATC tests compared to PC tests. However, as has been shown previously, ATC tests can underestimate the solder joint fatigue life in benign environments and may lead to costly, over-designed solutions. The AF developed in this work can be used to relate ATC test to PC tests so that ATC test can still be performed without being over conservative. The following example illustrates how to determine the required number of ATC qualification cycles based on PC field life requirements.

According to Gerke and Kromman [160] desktops may average a ΔT of 30°C four times per day. Using Eq. (10.5), this translates to a deskop power cycling field of 21472 cycles (10 years) at 1% failure for Case 3 in Table 10-3. The developed AF in Eq. (10.6) is used to determine the required number of 0/100°C 3cph ATC cycles at 50% failure to qualify the CBGA for 10 years of 30/60°C 0.25 cph at 1% failure. The resulting AF of 20.6x from Eq. (10.6) requires a mean fatigue life, N_{50}, of 1041 cycles (15 days) at 0/100C 3cph ATC to achieve the desired 10 years of life at 1% failure. In comparison, the Norris-

Landzberg AF of 4.6 times results in a longer ATC qualification time of 65 days (4667 cycles). This four fold increase in ATC cycles may unnecessarily lengthen the qualification process and may result in discarding legitimate designs. Table 10-6 summarizes the results and shows that the Norris-Landzberg AF is overly conservative compared to the design based AF and may lead to costly over designed thermal solutions or discarding sufficient designs [50].

Table 10-6. Number of ATC cycles to qualify a package (case 3) for a given desktop field life.

Desired desktop power cycling field life	ATC cycles to qualify based on developed AF	ATC cycles to qualify based on Norris-Landzberg AF
$N_{1\%}$ PC [30/60°C.25 cph]	N_{50} ATC [0/100°C 3cph]	N_{50} ATC [0/100°C 3cph]
21472 (10 years)	1041 (15 days)	4667 (65 days)

Figure 10-3 gives AF's for Cases 2, 3, and 4 of Table 10-3 against five different ATC/PC environments. Master et al. [161] presents environment conditions for desktops and laptops: Desktops operate at 25-65^{o}C at 1-1.5 cycles/day and should survive 1250-1875 cycles, 5 yr. life at 100ppm failure; laptops operate at 25-55^{o}C at 8 cycles/day and should survive 10,000 cycles, 5 yr. life at 100ppm failure. Figure 7 shows that the fairly benign laptop environment (ΔT = 30°C, 8 times a day) has the largest AF's due to the low thermal excursion at T_j and short amount of dwell time for long term creep damage to occur. For the desktop environment with ΔT = 40°C at 1 cycle a day the longer cycles and slightly higher temperatures allow more creep damage to occur than in the laptop environment. Design factors play a large role in determine the AF in fairly benign environments. As can be seen from the fourth column in Figure 10-3, the AF varies from 432x for a thick HICTE package all the way down to 75x for a thin alumina ceramic package. The Norris-Landzberg AF is 35x, no matter what design parameters are used.

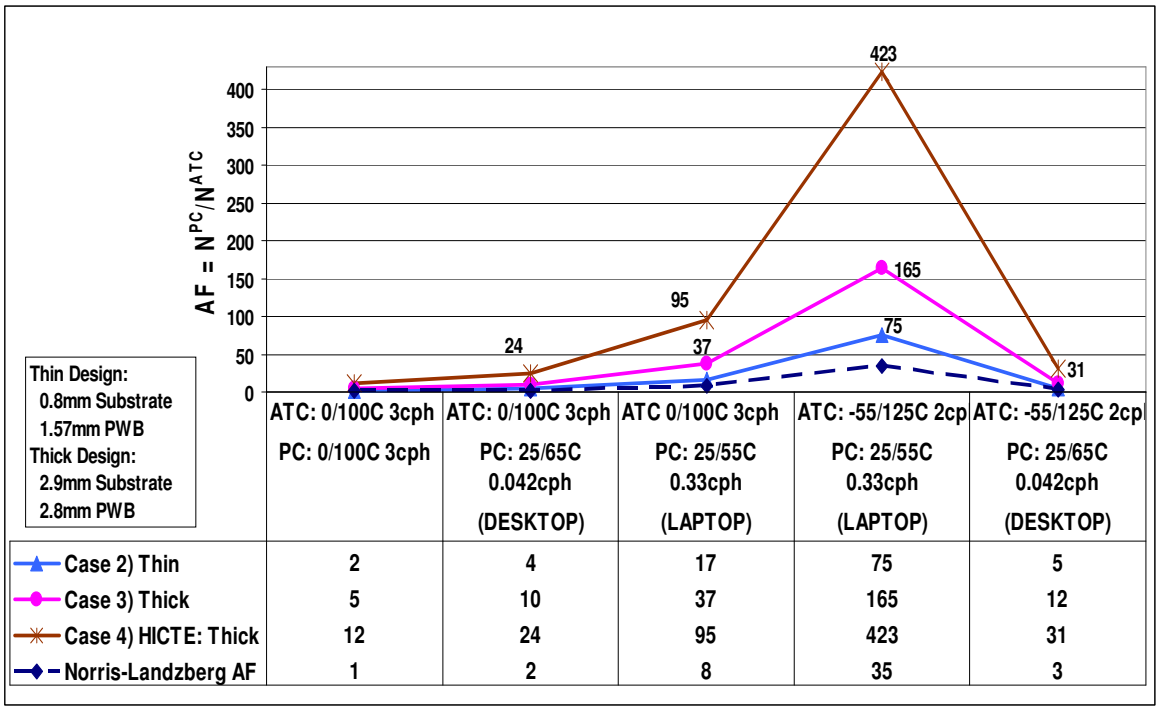


Figure 10-3. Design based AF for several common ATC and PC environments at 50% failure.

10.6. CONCLUSIONS

Design-based predictive solder joint fatigue life equations for ATC and PC were developed using literature ATC experiments, FEM, laser moiré interferometry, DOS, regression analysis, the Norris-Landzberg AF, and the Weibull distribution. The design parameters are substrate thickness, substrate conductivity, PWB thickness, and CTE mismatch between the substrate and PWB. The predictive equations allow for quick assessment of CBGA solder joint fatigue life [162] for designers without expertise in FEM or reliability analysis. The predictive equations can be implemented into the design process early on so designers can influence solder joint reliability early on.

An Acceleration Factor for relating ATC test to PC tests with consideration of proper design parameters was developed and compared to the Norris-Landzberg Acceleration Factor. Design parameters such as the substrate conductivity and CTE mismatch were found to have large effects on the AF.

The method for developing the design based AF for solder joint fatigue can also be applied to decoupling capacitors, thermal interface materials, die cracking, and other damage mechanisms.

CHAPTER 11

INVESTIGATION OF SOLDER JOINT FATIGUE FAILURE UNDER SEQUENTIAL THERMAL AND VIBRATION ENVIRONMENTS

11.1. INTRODUCTION

Thus far, this work has developed unified finite-element modeling methodology and has applied the methodology to thermal cycling or power cycling or vibratino loading conditions, and has validated the results from the models against experimetnal data. As discussed earlier, thermal cycling and power cycling conditions create low-cycle fatige conditions, while vibration loading creates high-cycle fatigue conditions. In actual applications both low cycle (thermal cycling and power cycling) as well as high-cycle (vibration) conditions exist, and therfore, it is essential to understand the effect of both on solder joint fatigue damage. As a first step, one way to address this is to run sequential thermal cycling and vibration loading experiments and understand the evolution of solder damage. Accordingly, this chapter develops a nonlinear cumulative damage rule based on Eq. (4.12) for CCGA's under two types of sequential loading: T-V (thermal and then vibration) loading, and V-T (vibration then thermal loading) such that Eq. (4.12) becomes Eq. (11.1):

$$CDI = 1.0 = \left(\frac{n_T}{N_T}\right)^{m_T} + \left(\frac{n_V}{N_V}\right)^{m_V} \tag{11.1}$$

where n is the actual number of applied cycles, N is the number of cycles to failure, m is a fitting parameter that varies for each load type and on the sequence of loads, and the subscripts T and V refer to thermal and vibration loading respectively. The fixed value of 1.0 on the left hand side of the the equation represents the cumulative damge index CDI, and is also called the total fatige life ratio. For the purposes of determining m_T and m_V during regresion analysis, the CDI is set equal to 1.0. The values of m_T and m_V vary depending on whether the sequence of loading is T-V or V-T. Single environment tests

allow for determination of the number of cycles to failure N_i under the ith step loading. Accelerated thermal cycle tests at -25/105°C at 2cph were performed to determine N_T as described in section 7.3.1. Sinusoidal out-of-plane vibration tests were performed to determine N_V as described in section 8.1 where an input acceleration of 1G is driven at the fundamental frequency of the system.

The details of the sequential T-V and V-T tests and development of the nonlinear cumulative damage rule of Eq. (4.12) is now described.

11.2. SEQUENCE TESTS

The first step of the sequence T-V was performed in this manner such that approximately one half of the expected fatigue life N_T was consumed, i.e. $n_T/N_T \approx 0.5$. The first step of the sequence V-T test was performed such that approximately one quarter of the expected fatigue life N_V was consumed, i.e. $n_V/N_V \approx 0.25$. The value of 0.25 was to ensure that no test vehicles failed before being subjected to the ATC step of the sequential V-T test. Due to the difficulty in stopping the test at preciseltest at a fatigue life ratio of precisely 0.25, there is a small distribution around the fatigue life ratio of 0.25. After the desired ratio of fatigue life n_1/N_1 is performed in the first step, then the second step is performed until solder joint failure occurs. The fatigue life ratio n_{21}/N_2 is then recorded and the *CDI* value is calculated.

Table 11-1 presents the results for the T-V and V-T sequential load tests. For T-V sequential steps step 1 is thermal and step 2 is vibration, likewise, for V-T loading step 1 is vibration and step 2 is thermal.

The *CDI* as shown in Table 11-1 should be the same for either sequence of loading T-V or V-T if sequence of loading has no effect. There is a distribution to the *CDI* so the median value of the distribution will be taken to represent the *CDI* . It can be seen that the median value for loading T-V is 0.66 and the median value for loading V-T is 0.96.

The median value for the *CDI* of the T-V sequence is lower than the V-T sequence, which indicates that the T-V sequence is a harsher sequence than V-T.

Table 11-1. Results of Sequential T-V and V-T tests.

T-V Load Sequence					
n_1	n_1/N_1	n_2	n_2/N_2		*CDI* $(n_1/N_1 + n_2/N_2)$
800	0.50	6.93E4	0.04		0.54
800	0.50	1.15E5	0.06		0.57
800	0.50	1.35E5	0.07		0.58
800	0.50	2.86E5	0.16		0.66
800	0.50	3.38E5	0.19		0.69
800	0.50	8.94E5	0.49		0.99
800	0.50	9.84E5	0.54		1.04
				Mean	0.73
				Median	0.66
				Range	0.50
V-T Load Sequence					
n_1	n_1/N_1	n_2	n_2/N_2		*CDI* $(n_1/N_1 + n_2/N_2)$
4.35E5	0.24	23	0.01		0.25 (outlier-not included)
4.15E5	0.23	24	0.02		0.25 (outlier-not included)
5.76E5	0.32	890	0.56		0.88
5.33E5	0.29	1000	0.63		0.92
5.40E5	0.30	1100	0.69		0.99
4.19E5	0.23	1300	0.82		1.05
				Mean	0.96
				Median	0.96
				Range	0.17

The first two data points of the V-T sequence in Table 11-1 were determined to be outliers due to an excessive vibration loading during testing which caused premature thermal cycling failure.

A nonlinear cumulative damage law to investigate the sequence effect will now be developed to account for the sequence affect and difference in damage mechanisms between thermal cycling and vibration..

11.3. NONLINEAR CUMULATIVE DAMAGE RULE

Nonlinear cumulative damage models according to Eq. (11.1) were developed for each load sequence using the median values and single step tests. The parameter fitting

exponents are found to be $m_T = 0.47$ and $m_V = 0.70$ for the T-V sequential tests, and $m_T = 0.91$ and $m_V = 0.93$ for the V-T sequential tests as shown in equations (11.2) and (11.3) respectively.

T-V Sequence $$CDI = \left(\frac{n_T}{N_T}\right)^{0.47} + \left(\frac{n_V}{N_V}\right)^{0.70} \quad (11.2)$$

V-T Sequence $$CDI = \left(\frac{n_T}{N_T}\right)^{0.91} + \left(\frac{n_V}{N_V}\right)^{0.93} \quad (11.3)$$

The closer an exponent is to a value of 1.0 the less of an effect it has the cumulative damage fatigue life ratio. By comparing $m_T = 0.47$ form the T-V test and $m_V = 0.93$ from the V-T test, it can be seen that performing the thermal step first is more damaging than performing the vibration step first. From a physical damage perspective, the sequence effect may be explained by looking at crack initiation and crack propagation for each sequence T-V and V-T. As noted in the single step tests, thermal cycling tends to initiate cracks more quickly or at a lower ratio of n_i/N_i. Depending upon the dynamic boundary conditions, crack initiation tends to occur more quickly under thermal loading than vibration loading. This is due to the fact that under thermal loads the solder microstructure is degraded and the solder joint deforms significantly into an S-shape as noted previously. Thus, under T-V testing, subsequent failure under vibration loading in the second step occurs quickly as a crack is preexisting and crack growth can occur. More experimental testing focused on observing crack initiation and crack propagation percentage as a function of n_i/N_i could help further explain the sequence effect from a crack initiation and propagation perspective.

Figure 11-1 plots the damage fractions for each step and compares them to the linear cumulative damage rule and the non-linear cumulative damage rule.

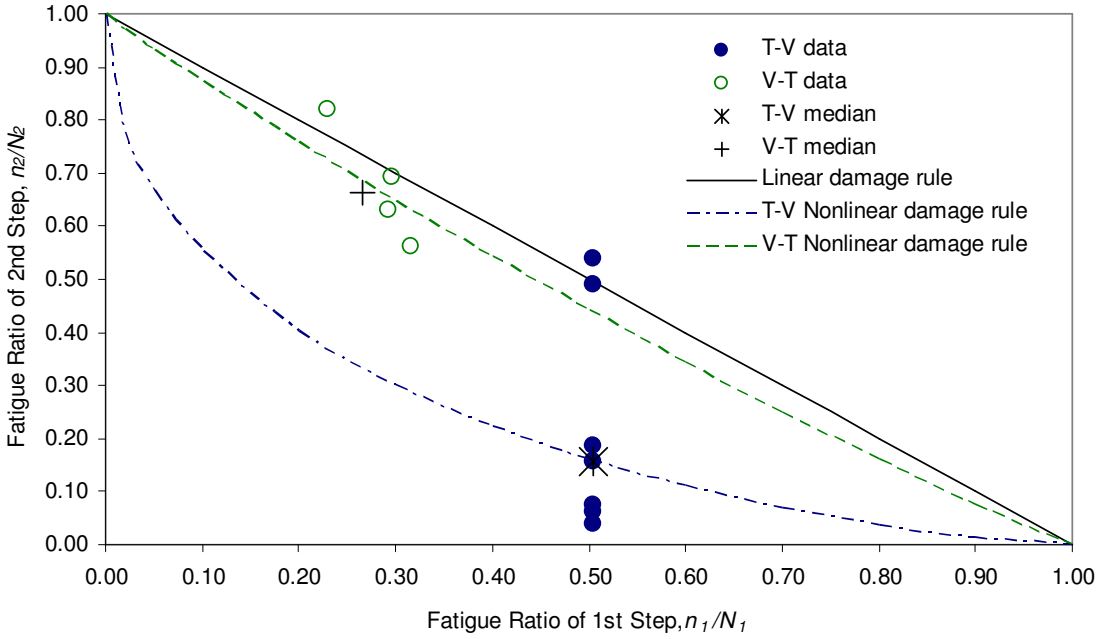


Figure 11-1. Plot of n_1/N_1 vs n_2/N_2 for sequential loadings T-V (thermal followed by vibration) and V-T (vibration followed by thermal) along with linear and nonlinear damage models.

It can be seen in Figure 11-1 that the linear damage rule overestimates fatigue life for both sequences of loading, just slightly for the V-T loading, but severely for the T-V case. The nonlinear damage rule provides a good fit to the experimental data. More experiments run at various fatigue life ratios should be run to gain better confidence in the models.

11.4. DISTRIBUTION OF THE NONLINEAR CUMULATIVE DAMAGE INDEX

Just as a distribution for the linear *CDI* from Miner's rule was observed in Table 11-1, a distribution for the nonlinear *CDI* of Eq. (11.2) and Eq. (11.3) can be observed. Using the same experimental data as presented in Table 11-1, the linear *CDI* and nonlinear *CDI* is given in Table 11-2.

Table 11-2. Comparison of linear and nonlinear *CDI* distributions

n_1/N_1	n_2/N_2		T-V Load Sequence Linear *CDI* $(n_1/N_1 + n_2/N_2)$	Nonlinear *CDI*. Eq. (11.2) $((n_1/N_1)^{m1} + (n_2/N_2)^{m2})$
0.50	0.04		0.54	0.83
0.50	0.06		0.57	0.87
0.50	0.07		0.58	0.88
0.50	0.16		0.66	1.00
0.50	0.19		0.69	1.03
0.50	0.49		0.99	1.33
0.50	0.54		1.04	1.37
		Mean	0.73	1.00
		Median	0.66	0.99
		Range	0.50	0.55

n_1/N_1	n_2/N_2		V-T Load Sequence *CDI* $(n_1/N_1 + n_2/N_2)$	Nonlinear *CDI*. Eq. (11.3) $((n_1/N_1)^{m1} + (n_2/N_2)^{m2})$
0.32	0.56		0.88	0.93
0.29	0.63		0.92	0.98
0.30	0.69		0.99	1.04
0.23	0.82		1.05	1.09
		Mean	0.96	1.01
		Median	0.96	1.01
		Range	0.17	0.16

As shown in Table 11-2, the median value of the the nonlinear *CDI*s are 0.99 and 1.01 for the T-V and V-T loading sequences respectively. It is expected that the nonlinear *CDI* median values for T-V and V-T loading sequences should be equivalent and equal to 1.0 because the sequence effect is characterized. In contrast, the linear *CDI* median values of 0.66 for T-V and 0.96 for V-T differ significantly and do not account for the sequence effect as observed previously.

The range of *CDI* for the T-V loading sequence ranges from a minimum of 0.83 to a maximum of 1.37. To be on the conservative side for safety considerations, it would be reasonable to assume failure to occur when the nonlinear *CDI* for the T-V sequences reaches 0.83. Likewise, the V-T nonlinear *CDI* ranges over a smaller range of 0.93 to 1.09, and a conservative safety estimate of the nonlinear *CDI* for V-T sequences could be 0.93. However, more experimental data should be performed to get a better characterization for the nonlinear *CDI* distribution.

11.5. EXTENSION OF NONLINEAR SEQUENTIAL CUMULATIVE DAMAGE RULE TO INCLUDE POWER CYCLING (PC)

The developed nonlinear sequential cumulative damage rule can be expanded to include PC. In Eq. (7.2) and Eq. (7.4) the fatigue life model developed for PC is the same as ATC. The damage mechanism under PC is the same as ATC. Therefore, the PC damage ratio n_P/N_P can be used in place of the ATC damage ratio n_T/N_T in equations (11.2) and (11.3). Equations (11.4) and (11.5) show the two sequence equations for P-V loading (power cycling followed by vibration) and V-P loading (vibration followed by power cycling).

P-V Sequence
$$1.0 = \left(\frac{n_P}{N_P}\right)^{0.47} + \left(\frac{n_V}{N_V}\right)^{0.70} \tag{11.4}$$

V-P Sequence
$$1.0 = \left(\frac{n_P}{N_P}\right)^{0.91} + \left(\frac{n_V}{N_V}\right)^{0.93} \tag{11.5}$$

Additionally, the nonlinear sequential cumulative damage rule can be further expanded to include the loading sequences of T-P-V and V-T-P. This is based on the fact that ATC and PC share the same damage mechanism and solder joint failure equation, therefore the damage ratios n_T/N_T and n_P/N_P share the same exponent. The equations for T-P-V and V-P-T sequential loading are shown in equation (11.6) and equation (11.7) respectively.

T-P-V Sequence
$$1.0 = \left(\frac{n_T}{N_T} + \frac{n_P}{N_P}\right)^{0.47} + \left(\frac{n_V}{N_V}\right)^{0.70} \tag{11.6}$$

V-T-P Sequence
$$1.0 = \left(\frac{n_T}{N_T} + \frac{n_P}{N_P}\right)^{0.91} + \left(\frac{n_V}{N_V}\right)^{0.93} \tag{11.7}$$

11.6. CONCLUSIONS

In this work, the sequence effect on solder joint reliability of a CCGA component under sequential accelerated thermal cycling tests (ATC) and vibration was investigated. It was determined that the T-V sequence (thermal cycling followed by vibration loading) was a harsher sequence than the V-T sequence (vibration loading followed by thermal cycling). The difference was attributed to the severe deformation and microstructural changes that

occur in thermal cycling which initiate cracks quickly and quicken the subsequent vibration loading.

A simple nonlinear cumulative damage model was developed to account for the sequence effect for sequential thermal cycling and vibration loading of a CCGA electronic component. The nonlinear cumulative damage model can be used to predict remaining fatigue life for a component that has experienced some level of damage from a prior environment, such as transportation or preconditioning. In addition, the model was extended to include power cycling as another environment in the sequential loading.

The methodology, developed in this work, has the potential for application for other electronic packages and environments.

CHAPTER 12

RESEARCH CONTRIBUTIONS AND FUTURE WORK

12.1. RESEARCH CONTRIBUTIONS

This work has made important research contributions in the area of solder joint reliability as listed below:

- This work has developed a unified modeling methodology to study solder joint fatigue under thermal cycling, power cycling, and vibration loading conditions. The developed methodology is able to accommodate the time- and temperature-dependent material behavior and material damage index when the packages are subjected to thermal cycling, power cycling, and vibration loading conditions. The developed methodology is able to account for solder joint geometry such that both vibration-related parameters as well as TC and PC-related parameters can be obtained.
- This work has employed the unified modeling methodology to develop universal polynomial predictive equations for thermal cycling and power cycling. The developed predictive equations are grounded in the mechanics of material behavior and at the same are easy enough to be used by a wide range of engineers and experimentalists without extensive background in mechanics and/or finite-element modeling.
- This work has determined acceleration factors associated with power cycling and thermal cycling, and has produced a unique formulation for the determination of acceleration factors. Given the same temperature extremes and package geometry, PC tests and ATC tests will give different fatigue lives. The developed AF takes into account the difference between the ATC tests that do not have thermal gradients in the packaging assembly, and PC tests that have thermal gradients in the packaging assembly. The proposed equations are grounded in mechanics of material behavior and are void of simplistic assumptions used by industry
- This work has used the unified modeling methodology to determine cumulative damage in solder joints under thermal cycling and vibration load combinations, and has validated the results using first-of-its experimental data.

This work has contributed to the understanding of solder joint reliability under thermal cycling, power cycling, and vibration loading. In particular, this work has:

1) Effectively included plasiticity, creep, and thermal properties in equivalent beam models such that the mechanical behavior of every solder joint in a large area array electronic package is accounted for properly. This is the first known study to include creep in the equivalent beam method.

2) Demonstrated a unified 3D finite element modeling capable of capturing the correct mechanical and thermal behaviors experienced under thermal cycling, power cycling, and vibration loading. The mechanical behavior and thermal behavior of the unified 3D finite element model were validated against laser moiré interferometry, cross-section analysis, and dye-and-pry analysis.

3) Developed fatigue equations for 90Pb10Sn solder for both high cycle vibration failure and low cycle ATC/PC. This study has developed the first known fatigue equation of 90Pb10Sn solder under high cycle vibration loading.

4) Demonstrated a methodology for developing universal fatigue life prediction equations that are easy-to-use and do not require expensive software or advanced knowledge of solder joint fatigue and modeling.

5) Developed an AF for relating ATC tests to PC tests for CBGAs. The developed AF can be used to help prevent expensive over design of components. Additionally, ATC tests can be performed in place of expensive and hard-to-design PC tests.

6) Developed a nonlinear cumulative damage law to account for the nonlinearity and effect of sequence loading under thermal cycling, power cycling, and vibration loading.

7) Demonstrated the importance of considering all environments an electronic package may experience.

12.2. FUTURE WORK

The following are recommendations for future work in this area

1) The nonlinear sequence cumulative damage rule should be verified with more samples at different damage ratios of n_1/N_1.

2) Random vibration loading needs to be included in place of sinusoidal out-of-plane vibration loading. Random vibration excites multiple fundamental modes at once and is more realistic of an actual field environment. The difficulty with random vibration lies in the modeling work and predicting where damage will occur.

3) This study used components containing Pb-based solder. Understanding of Pb-free solders under multiple environments needs to be understood. The work should be extended to Pb-free PBGAs. The exact same methodologies used in this study will be applicable to any other component. The finite element modeling will be a little more difficult when underfill is included due to the equivalent beams not being true SOLID elements.

4) Combined environmental loading of thermal and vibration loading needs to be understood. The experiments can be performed in a thermal chamber that is coupled with an electrodynamic shaker. The difficulty will be in coupled modeling of the thermal cycling and vibration loading. The time scales are orders of magnitude different which makes it difficult to simulate in an FEM.

VITA

Andrew E. Perkins

PERKINS was born in South Portland, Maine. He completed a Dual Degree program in 2000, receiving a Bachelors of Natural Science:Pre-engineering from Covenant College and Bachelor of Science in Mechanical Engineering from The Georgia Institute of Technology. When not working on microelectronics packaging reliability, he enjoys reading books of nearly any subject, hiking and mountain biking nearly any terrain, and nurturing his wife and children.

REFERENCES

[1] Tummala, R.R., Rymaszewski, E.J., and Klopfenstein, A.G., eds. *Microelectronics Packaging Handbook*. 2 ed. 1998, Kluwer Academic Pub.

[2] Brown, W.D., ed. *Advanced Electronic Packaging with Emphasis on Multichip Modules*. ed. W.D. Brown. 1998, IEEE Press: New York.

[3] Suhir, E., "Stresses in bi-metal thermostats". *ASME Journal of Applied Mechanics*, 1986. 53(3): p. 657.

[4] Timeshenko, S., "Analysis of Bi-Metal Thermostats". *J. Optic. Soc. Am.*, 1925. 11: p. 233-255.

[5] Wen, Y. and Basaran, C. "An analytical model for thermal stress analysis of multi-layered microelectronics packaging". in *54th Electronic Components and Technology Conference*. 2004. Las Vegas, NV, USA: IEEE.

[6] Wong, T.E., Lau, C.Y., and Fenger, H.S., "CBGA solder joint thermal fatigue life estimation by a simple method". *Soldering and Surface Mount Technology*, 2004. 16(2): p. 41.

[7] Pang, J.H.L., Che, F.X., and Low, T.H. "Vibration fatigue analysis for FCOB solder joints". 2004. Las Vegas, NV, USA: IEEE.

[8] Syed, A. "A Review of Finite Element Methods for Solder Joint Analysis". in *Experimental/Numerical Mechancis in Electronic Packaging*. 1996: SEM.

[9] Pang, J.H.L. and Chong, D.Y.R., "Flip chip on board solder joint reliability analysis using 2-D and 3-D FEA models". 2001. 24(2): p. 499.

[10] Lee, S.B. and Ham, S.J. "Fatigue life assessment of bump type solder joint under vibration environment". in *InterPACK '99*. 1999.

[11] Cheng, H.-C., Yu, C.-Y., and Chen, W.-H. "Effective Thermal-mechanical Modeling of Solder Joints". in *ASME IMECE2002*. 2002.

[12] Syed, A. "Predicting solder joint reliability for thermal, power, and bend cycle within 25% accuracy". in *51st Electronic Components and Technology Conference*. 2001. Orlando, FL, USA: IEEE.

[13] Corbin, J.S., "Finite Element Analysis for Solder Ball Connect (SBC) Structural Design Optimization". *IBM Journal of Research and Developments*, 1993. 37(5): p. 585-96.

[14] Rodgers, B., Punch, J., and Jarvis, J. "Finite Element Modelling of a BGA Package Subjected To Thermal and Power Cycling". in *ITHERM 2002*. 2002. San Diego, CA, USA: IEEE.

[15] IPC, *Guidelines for Accelerated Reliability Testing of Surface Mount Attachments, IPC-SM-785*. 1992, Institute of Interconnecting and Packaging Electronic Circuits: Northbrook, IL.

[16] Han, B., et al., "Verification of numerical models used in microelectronics packaging design by interferometric displacement measurement methods". *ASME Journal of Electronic Packaging*, 1996. 118(3): p. 157.

[17] Wang, J., et al., "Creep behavior of a flip-chip package by both FEM modeling and real time moire interferometry". *ASME Journal of Electronic Packaging*, 1998. 120(2): p. 179.

[18] Han, B., Post, D., and Ifju, P., "Moire interferometry for engineering mechanics: Current practices and future developments". *Journal of Strain Analysis for Engineering Design*, 2001. 36(1): p. 101.

[19] Verma, K., et al., "On the design parameters of flip-chip PBGA package assembly for optimum solder ball reliability". *IEEE Transactions on Components and Packaging Technologies*, 2001. 24(2): p. 300.

[20] Darveaux, R., "Crack initiation and growth in surface mount solder joints". 1993. 2105: p. 86.

[21] Norris, K.C. and Landzberg, A.H., "Reliability of Controlled Collapse Interconnections". *IBM Journal of Research and Developlment*, 1969. 13(3): p. 266.

[22] Kromann, G.B., "Thermal Modeling and Experimental Characterization of the C4/Surface-Mount-Array Interconnect Technologies". *IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A*, 1995. 18(1): p. 87.

[23] Bar-Cohen, A. and Krueger, W.B. "Thermal Characterization of Chip Packages-Evolutionary Development of Compact Models". in *Thirteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*. 1997. Austin, TX, USA: IEEE.

[24] Vinke, H. and Lasance, C.J.M., "Compact models for accurate thermal characterization of electronic parts". *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, 1997. 20(4): p. 411.

[25] Lasance, C.J.M., "The influence of various common assumptions on the boundary-condition-independence of compact thermal models". *IEEE Transactions on Components and Packaging Technologies*, 2004. 27(3): p. 523.

[26] Zemo, Y. and Young, K. "Validation study of compact thermal resistance models of IC packages". in *46th ECTC*. 1996. Orlando, FL, USA: IEEE.

[27] Sundararajan, R., McCluskey, P., and Azarm, S. "Semi analytic model for thermal fatigue failure of die attach in power electronic building blocks". in *1998 Fourth International High Temperature Electronics Conference. HITEC*. 1998. Albuquerque, NM, USA: IEEE.

[28] DeVoe, J., Ortega, A., and Berhe, M. "On the performance of compact thermal models of electronic chip packages in conjugate board level simulation". in *Nineteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*. 2003. San Jose, CA, USA: IEEE.

[29] Hong, B.Z. and Yuan, T.-D., "Heat transfer and nonlinear thermal stress analysis of a convective surface mount package". *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, 1997. 20(2): p. 213.

[30] Hong, B.Z. and Yuan, T.-D., "Integrated Flow-Thermomechanical Analysis of Solder Joints Fatigue in a Low Air Flow C4/CBGA Package". *International Journal of Microcircuits and Electronic Packaging*, 1998. 21(2): p. 137.

[31] Gektin, V., et al. "Substantiation of numerical analysis methodology for CPU package with non-uniform heat dissipation and heat sink with simplified fin modeling". in *Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena In Electronic Systems*. 2004. Las Vegas, NV, USA: IEEE.

[32] Ramakrishna, K. and Lee, T.Y.T. "Prediction of Thermal Performance of Flip Chip-Plastic Ball Grid Array (FC-PBGA) Packages: Effect of Substrate Physical Design". in *Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*. 2002. San Diego, CA, USA: IEEE.

[33] Lohan, J., et al. "Using experimental analysis to evaluate the influence of printed circuit board construction on the thermal performance of four package types in both natural and forced convection". in *ITHERM 2000*. 2000. Las Vegas, NV, USA: IEEE.

[34] Shabany, Y. "Component size and effective thermal conductivity of printed circuit boards". in *Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*. 2002. San Diego, CA, USA: IEEE.

[35] Yuan, T.-D., et al. "Thermal Management for High Performance Integrated Circuits with Non-Uniform Chip Power Considerations". in *Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*. 2001. San Jose, CA, USA: IEEE.

[36] Towashiraporn, P., et al., "Predictive reliability models through validated correlation between power cycling and thermal cycling accelerated life tests [package solder joints]". *Soldering & Surface Mount Technology*, 2002. 14(3): p. 51.

[37] Ham, S.J., Cho, M.S., and Lee, S.B. "Thermal Deformations of CSP Assembly During Temperature Cycling and Power Cycling". in *International Symposium on Electronic Materials and Packaging*. 2000. Hong Kong, China: IEEE.

[38] Wakil, J.A. and Ho, P.S., "Simulating Package Behavior under Power Dissipation using Uniform Thermal Loading". *IEEE Transactions on Advanced Packaging*, 2001. 24(1): p. 60.

[39] Andrews, J.A., "Package Thermal Resistance Model: Dependency on Equipment Design". *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 1988. 11(4): p. 528.

[40] Rosten, H.I., Lasance, C.J.M., and Parry, J.D., "The world of thermal characterization according to DELPHI-Part I: Background to DELPHI". *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, 1997. 20(4): p. 384.

[41] Lasance, C.J.M., Rosten, H.I., and Parry, J.D., "The world of thermal characterization according to DELPHI-Part II: Experimental and numerical methods". *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, 1997. 20(4): p. 392.

[42] Wakil, J. and Ho, P.S. "Effect of nonuniform temperature on thermal modeling and strain distribution in electronic packaging". in *49th Electronic Components and Technology Conference*. 1999. San Diego, CA, USA: IEEE.

[43] Kromann, G.B., Gerke, D., and Huang, W. "Motorola's PowerPC 603 and PowerPC 604 RISC Microprocessor: The C4/Ceramic-Ball-Grid Array Interconnect Technology". in *45th Electronic Components and Technology Conference*. 1995. Las Vegas, NV, USA: IEEE.

[44] Gerke, R.D. and Kromann, G.B. "The Effect of Solder-joint Temperature Rise on Ceramic-Ball-Grid Array to Board Interconnection Reliability: The Motorola PowerPC 603 and PowerPC 604 Microprocessors and MPC105 Bridge/Memory Controller". in *Proceedings of the International Electronic Packaging Conference - INTERpack '95*. 1995. Lahaina, HI, USA: ASME.

[45] Engelmaier, W., "Fatigue life of leadless chip carrier solder joints during power cycling". *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 1983. CHMT-6(3): p. 232.

[46] Davitt, E., Stam, F.A., and Barrett, J., "The effect of power cycling on the reliability of lead-free surface mount assemblies". *IEEE Transactions on Components and Packaging Technologies*, 2001. 24(2): p. 241.

[47] Ahmed, I.Z. and Park, S.B. "An Accurate Assessment of Interconnect Fatigue Life through Power Cycling". in *The Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena In Electronic Systems*. 2004. Las Vegas, NV, USA: IEEE.

[48] Park, S.B., Joshi, R., and Sammakia, B. "Thermomechanical Behavior of Organic and Ceramic Flip Chip BGA Packages Under Power Cycling". in *ITHERM 2005*. 2005. San Jose, CA, USA: IEEE.

[49] Martin, G.B., et al. "Real World Fatigue Life of Ceramic Surface Mount Packages: The Power Cycling Advantage". in *2000 Semicon West*. 2000.

[50] Syed, A. and Doty, M. "Are We Over Designing for Solder Joint Reliability? Field vs. Accelerated Conditions, Realistic vs. Specified Requirements". in *49th Electronic Components and Technology Conference*. 1999. San Diego, CA, USA: IEEE.

[51] Galloway, J.E., et al. "Analysis of acceleration factors used to predict BGA solder joint field life". in *Surface Mount Technology Association International Conference*. 2001. Rosemont, IL, USA: Surface Mount Technol. Assoc.

[52] Cole, M.S., Kastberg, E.J., and Martin, G.B. "Shock and vibration limits for CBGA and CCGA". in *SMI. Surface Mount International.* 1996. San Jose, CA, USA: Surface Mount Technol. Assoc.

[53] Barker, D.B., Chen, Y.S., and Dasgupta, A., "Estimating the Vibration Fatigue Life of Quad Leaded Surface Mount Components". *ASME Journal of Electronic Packaging*, 1993. 115(2): p. 195.

[54] McMurray, K.E. and Mitchell, L., "Characterization of Boundary-Conditions for Wedge-lock-mounted Printed Circuit Boards". *Advanced Electronic Packaging*, 1997. 19(2): p. 1321-1327.

[55] Steinberg, D.S., Preventing Thermal Cycling and Vibration Failures in Electronic Equipment. 2001, New York: Wiley.

[56] Suhir, E. "Could Compliant External Leads Reduce the Strength of a Surface Mounted Device?" in *38th Electronic Components and Technology Conference*. 1988.

[57] Suhir, E., "Is the Maximum Acceleration an Adequate Criterion of the Dynamic Strength of a Structural Element in an Electronic Package?" *IEEE Transactions on Components, packaging, and manufacturing Technology, Part A*, 1997. 20(4): p. 513-517.

[58] Singal, R.K. and Gorman, D.J., "A general analytical solution for free vibration of rectangular plates resting on fixed supports and with attached masses". *ASME Journal of Electronic Packaging*, 1992. 114(2): p. 239.

[59] Pitarresi, J.M., et al., "The `smeared' property technique for the FE vibration analysis of printed circuit cards". *ASME Journal of Electronic Packaging*, 1991. 113(3): p. 250.

[60] Hsu, S.M., Lin, J.C., and Chiang, K.N. "A Full-Scale 3D Finite Element Analysis for No-underfill Flip Chip Packages". in *ASME International Mechanical Engineering Congress & Exposition*. 2002. New Orleans, LA.

[61] Yang, Q.J., et al., "Reliability of PBGA assemblies under out-of-plane vibration excitations". *EEE Transactions on Components and Packaging Technologies*, 2002. 25(2): p. 293.

[62] Che, F.X., et al. "Vibration Fatigue Test and Analysis for Flip Chip Solder Joints". in *5th Electronics Packaging Technology Conference*. 2003. Singapore: IEEE.

[63] Perkins, A. and Sitaraman, S.K. "Vibration-induced Solder Joint Failure of a Ceramic Column Grid Array (CCGA) package". in *54th Electronic Components and Technology Conference*. 2004. Las Vegas, NV, USA: IEEE.

[64] Pitarresi, J.M. and Primavera, A.A., "Comparison of modeling techniques for the vibration analysis of printed circuit cards". *ASME Journal of Electronic Packaging*, 1992. 114(4): p. 378.

[65] Pitarresi, J., et al. "Dynamic modeling and measurement of personal computer motherboards". in *52nd Electronic Components and Technology Conference*. 2002. San Diego, CA, USA: IEEE.

[66] Li, R.S. "Finite Element Modeling of Ball Grid Array Packages in System Packaging Vibration Analysis". in *NEPCON West - Fiberoptic Expo*. 2002.

[67] Wong, T.E., et al. "Development of BGA solder joint vibration fatigue life prediction model". in *49th Electronic Components and Technology Conference*. 1999. San Diego, CA, USA: IEEE.

[68] Yang, Q.J., et al., "Microelectronics reliability characterization of PBGA assemblies". *Microelectronics Reliability*, 2000. 40(7): p. 1097.

[69] Geng, P. and Beltman, W.M. "Monitoring Motherboard Shock Strain Response near BGA Solder Joints". in *SMTA International*. 2002. Rosemont Illionois.

[70] Nickerson, M.D. and Desai, C.S. "Design and reliability in electronic packaging including power temperature cycling and vibration effects". in *IPACK '03*. 2003.

[71] Basaran, C., Cartwright, A., and Zhao, Y., "Experimental Damage Mechanics of Microelectronics Solder Joints under Concurrent Vibration and Thermal Loading". *International Journal of Damage Mechanics*, 2001. 10(2): p. 153.

[72] Zhao, Y., et al. "Inelastic behavior of microelectronics solder joints under concurrent vibration and thermal cycling". in *Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*. 2000. Las Vegas, NV, USA: IEEE.

[73] Ghaffarian, R. "Shock and thermal cycling synergism effects on reliability of CBGA assemblies". in *IEEE Aerospace Conference*. 2000.

[74] Miner, M.A., "Cumulative Fatigue Damage". *ASME Journal of Applied Materials*, 1945. 12(3): p. A159-A164.

[75] Lau, J.H., ed. *Ball grid aray technology*. 1995, McGraw-Hill. 636.

[76] Wen, L., Mon, G.R., and Ross, R.G., Jr. "Inconsistencies in the understanding of solder joint reliability physics". 1997. Orlando, FL, USA: Minerals, Metals & Materials Soc (TMS), Warrendale, PA, USA.

[77] Nose, H., et al., "Temperature and Strain Rate Effects on Tensile Strength and Inelastic Constitutive Relationship of Sn=Pb Solders". *ASME Journal of Electronic Packaging*, 2003. 125: p. 59-6.

[78] Dowling, N.E., Mechanical behavior of materials: engineering methods for deformation, fracture, and fatigue. 1993, Upper Saddle River, New Jersey: Prentice-Hall, Inc.

[79] McDowell, D.L., Miller, M.P., and Brooks, D.C., Unified creep-plasticity theory for solder alloys. 1153 ed. Fatigue of Electronic Materials ASTM STP 1153, ed. S.A. Schroeder and M.R. Mitchell. 1994, Philadelphia: American Society for Testing and Materials. 42.

[80] Syed, A. "Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints". in *54th Electronic Components and Technology Conference*. 2004. Las Vegas, NV, USA: IEEE.

[81] Stone, D., et al. "Mechanisms of damage accumulation in solders during thermal fatigue". in *36th IEEE Electronic Components and Technology Conference*. 1986: IEEE.

[82] Dasgupta, A., et al., "Solder creep-fatigue analysis by an energy-partitioning approach". *ASME Journal of Electronic Packaging*, 1992. 114(2): p. 152.

[83] Schubert, A., et al. "Thermo-mechanical properties and creep deformation of lead-containing and lead-free solders". 2001. Braselton, GA, USA: IEEE.

[84] Wong, B., Helling, D.E., and Clark, R.W., "Creep-rupture model for two-phase eutectic solders". *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, 1988. 11(3): p. 284.

[85] Xu, C., Gang, C., and Chang-Dong, N., "Uniaxial ratcheting behavior of 63Sn37Pb solder with loading histories and stress rates". *Materials Science & Engineering A (Structural Materials: Properties, Microstructure and Processing)*, 2006. 421(1-2): p. 238.

[86] Bor Zen, H. and Bunell, L.G., "Nonlinear finite element simulation of thermoviscoplastic deformation of C4 solder joints in high density packaging under thermal cycling". *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, 1995. 18(3): p. 585.

[87] Coffin, L.F., "A Study of the Effects of Cyclic Thermal Stresses on a Ductile Metal". *Transactions of ASME*, 1954. 76: p. 931-950.

[88] Vandevelde, B., et al. "Solder parameter sensitivity for CSP life-time prediction using simulation-based optimization method". 2001. Orlando, FL, USA: IEEE.

[89] Darveaux, R., "Effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction". *ASME Journal of Electronic Packaging*, 2002. 124(3): p. 147.

[90] Zhang, Q., Dasgupta, A., and Haswell, P. "Viscoplastic constitutive properties and energy-partitioning model of lead-free Sn3.9Ag0.6Cu solder alloy". in *53rd Electronic Components and Technology Conference*. 2003. New Orleans, LA, USA: IEEE.

[91] Lee, W.W., Nguyen, L.T., and Selvaduray, G.S., "Solder joint fatigue models: review and applicability to chip scale packages". *Microelectronics Reliability*, 2000. 40(2): p. 231.

[92] Dasgupta, A., Sharma, P., and Upadhyayula, K., "Micro-mechanics of fatigue damage in Pb-Sn solder due to vibration and thermal cycling". *International Journal of Damage Mechanics*, 2001. 10(2): p. 101.

[93] Sayama, T., et al. "Evaluation of microstructural evolution and thermal fatigue crack initiation in SN-AG-CU solder joints". 2003. IPACK '03.

[94] Stolkarts, V., Moran, B., and Keer, L.M. "Constitutive and damage model for solders". in *48th Electronic Components and Technology Conference*. 1998. Seattle, WA, USA: IEEE.

[95] Sharma, P. and Dasgupta, A. "The connection between microstructural damage modeling and continuum damage modeling for eutectic Sn-Pb solder alloys". in *ASME IMECE2002*. 2002. New Orleans, LA.

[96] Barker, D., et al., "Combined Vibrational and Thermal Solder Joint Fatigue-A Generalized Strain versus Life Approach". *ASME Journal of Electronic Packaging*, 1990. 112(2): p. 129.

[97] Chih-Kuang, L. and Hsuan-Yu, T., "Creep properties of Sn-3.5Ag-0.5Cu lead-free solder under step-loading". *Journal of Materials Science: Materials in Electronics*, 2006. 17(8): p. 577.

[98] Singh, A., "Development and validation of an S-N based two phase bending fatigue life prediction model". *Journal of Mechanical Design, Transactions of the ASME*, 2003. 125(3): p. 540.

[99] Jin, O., Lee, H., and Mall, S., "Investigation into cumulative damage rules to predict fretting fatigue life of Ti-6Al-4V under two-level block loading condition". *Journal of Engineering Materials and Technology, Transactions of the ASME*, 2003. 125(3): p. 315.

[100] Kwang Soo, K., Xu, C., and Jin, D., "Fatigue life prediction of type 304 stainless steel under sequential biaxial loading". *International Journal of Fatigue*, 2006. 28(3): p. 289.

[101] Basaran, C. and Chandaroy, R., "Thermomechanical Analysis of Solder Joints under Thermal and Vibrational Loading". *ASME Journal of Electronic Packaging*, 2002. 124(1): p. 60.

[102] Manson, S.S. and Halford, G.R., "PRACTICAL IMPLEMENTATION OF THE DOUBLE LINEAR DAMAGE RULE AND DAMAGE CURVE APPROACH FOR TREATING CUMULATIVE FATIGUE DAMAGE". *International Journal of Fracture*, 1981. 17(2): p. 169.

[103] Marco, S.M. and Starkey, W.L., "A concept of fatigue damage". *Trans. ASME*, 1954. 76(4): p. 627-632.

[104] Han, B., "Thermal stresses in microelectronics subassemblies: Quantitative characterization using photomechanics methods". *Journal of Thermal Stresses*, 2003. 26(6): p. 583.

[105] Post, D., Han, B., and Ifju, P., High Sensitivity Moire: Experimental Analysis for Mechanics and Materials. Mechanical Engineering Series. 1994, NY: Springer-Verlag.

[106] Bongtae, H. "Thermal stresses in microelectronics subassemblies: quantitative characterization using photomechanics methods". 2003. Blacksburg, VA, USA: Taylor & Francis.

[107] Han, B., "Deformation mechanism of two-phase solder column interconnections under highly accelerated thermal cycling condition: an experimental study". *Transactions of the ASME. Journal of Electronic Packaging*, 1997. 119(3): p. 189.

[108] Cho, S. and Han, B., "Observing Real-time Thermal Deformations in Electronic Packaging". *Experimental Techniques*, 2002. 26(3): p. 25.

[109] Thomson, W.T. and Dahleh, M.D., Theory of vibration with application. 5th ed. 1998, Upper Saddle River, N.J.: Prentice Hall.

[110] Ginsberg, J.H., Mechancial and Structural Vibrations, Theory and Applications. 1 ed. 2001, New York: Wiley.

[111] *ANSYS 8.1*, ANSYS INC.

[112] Vandevelde, B., et al., "Modified Micro-macro Thermo-mechanical Modelling of Ceramic Ball Grid Array Packages". *Microelectronics Reliability*, 2003. 43(2): p. 307.

[113] Saito, N., Sasaki, K., and Hata, N. "Efficient Stress and Displacement Analysis Method for Area-array Structures". 1999.

[114] Hong, B.Z. and Yuan, T.-D. "Heat Transfer and Nonlinear Thermal Stress Analysis of a Convective Surface Mount Package". in *Inter-Society Conference on Thermal Phenomena in Electronic Systems*. 1996. Orlando, FL, USA: IEEE.

[115] Zahn, B.A. "Solder Joint Fatigue Life Model Methodology for 63Sn37Pb and 95.5Sn4Ag0.5Cu Materials". 2003. New Orleans, LA, USA: IEEE.

[116] Xiang, D., et al. "High I/O Glass Ceramic Package PbFree BGA Interconnect Reliability". in *2005 IEEE Electronic Components Technology Conference*. 2005.

[117] Kyocera, *http://global.kyocera.com/prdct/semicon/ic_pkg/hitce.html*.(date accessed: 11/2006)

[118] Cole, M. and Caulfield, T., "Constant strain rate tensile properties of various lead based solder alloys at 0, 50, and 100 degrees C". *Scripta Metallurgica et Materialia*, 1992. 27(7): p. 903.

[119] Hong, B.Z. and Ray, S.K. "Ceramic column grid array technology with coated solder columns". in *50th Electronic Components and Technology Conference*. 2000. Las Vegas, NV, USA: IEEE.

[120] Stone, D.S., "The creep-fatigue interaction in solders and solder joints". *Transaction of the ASME Journal Of Electronic Packaging*, 1990. 112(2): p. 100-103.

[121] Wang, G.Z., et al., "Applying Anand model to represent the viscoplastic deformation behavior of solder alloys". *ASME Journal of Electronic Packaging*, 2001. 123(3): p. 247.

[122] Dudek, R., et al. "Thermo-mechanical reliability aspects and finite element simulation in packaging". in *5th Electronics Packaging Technology Conference*. 2003. Singapore: IEEE.

[123] Han, B., *Verification of numerical models used in microelectronics product development,* in *Handbook of Moire measurement*. 2004, Inst. of Phys. p. 153.

[124] Yuan, T.D. "Convection Modelling of Flip Chip and Wirebond Surface Mounted Modules". in *ITHERM 1996*. 1996. Orlando, FL, USA: IEEE.

[125] Master, R.N., et al. "High TCE Ball Grid Array for Single Chip Ceramic Packaging". in *Pan Pacific Microelectronics Symposium*. 2000. Maui, HI, USA: Surface Mount Technol. Assoc.

[126] IBM, *CBGA Surface Mount Assembly and Rework - User's Guide*. 2002.

[127] Martin, G.B., et al., "Substrate Thickness and CBGA Fatigue Life". *Surface Mount Technology*, 1998. 12(2): p. 102, 104, 106, 108.

[128] Cole, M.S., et al. "CBGA Fatigue Life Improvement". in *SEMICON West 1999*. 1999: SEMI.

[129] Darveaux, R. "Effect of simulation methodology on solder joint crack growth correlation". in *50th Electronic Components and Technology Conference*. 2000. Las Vegas, NV, USA: IEEE.

[130] *Microsoft Excel 2003*. 1985-2003.

[131] *JMP*. 1989-2005, SAS Institute Inc.: Cary, NC.

[132] Solomon, H.D. "Fatigue of 60/40 solder [joints]". 1986. Seattle, WA, USA: IEEE.

[133] Cole, M.S., et al., "CCGA design variables and their effects on reliability". *Circuits Assembly*, 2002. 13(1): p. 66.

[134] Cole, M.S., et al. "The new millennium for CCGA - beyond 2000 I/O". in *SMTA International*. 2001. Rosemont, IL, USA: Surface Mount Technol. Assoc.

[135] Zhang, L., et al. "Solder joint reliability model with modified darveaux's equations for the micro SMD wafer level-chip scale package family". in *2003 Electronic Components and Technology Conference*. 2003. New Orleans, LA.

[136] Sinha, A., isaacs, P., and Tofil, T. "Mechanical reliability Analysis of CCGA solder joints". in *Surface Mount International*. 1997. San Jose, CA.

[137] Modi, M., McCormick, C., and Armendariz, N. "New insights in critical solder joint location". 2005. Lake Buena Vista, FL, USA: IEEE.

[138] Cole, M.S., et al. "Compressive Load Effects on CCGA Reliability". in *SMTA International*. 2002. Chicago.

[139] Qiang, Y. and Shiratori, M. "Fatigue-strength prediction of microelectronics solder joints under thermal cyclic loading". in *10th Congress of the World Organisation of Systems and Cybernetics*. 1997. Bucharest, Romania.

[140] Li, Y. and Mahajan, R.L., "CBGA solder fillet shape prediction and design optimization". *Transactions of the ASME. Journal of Electronic Packaging*, 1998. 120(2): p. 118-22.

[141] Pang, J.H.L., Seetoh, C.W., and Wang, Z.P., "CBGA solder joint reliability evaluation based on elastic-plastic-creep analysis". 2000. 122(3): p. 255.

[142] Perkins, A. and Sitaraman, S.K. "Predictive Fatigue Life Equation for CBGA Electronic Packages based on Design Parameters". in *Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena In Electronic Systems*. 2004. Las Vegas, NV, USA: IEEE.

[143] Perkins, A. and Sitaraman, S.K. "Thermo-mechanical Failure Comparison and Evaluation of CCGA and CBGA Electronic Packages". in *53rd Electronic Components and Technology Conference*. 2003. New Orleans, LA, USA: IEEE.

[144] Xie, D.J. and Wang, Z.P., "Process capability study and thermal fatigue life prediction of ceramic BGA solder joints". 1998. 30(1-2): p. 31.

[145] Burnette, T., et al. "Underfilled BGAs for ceramic BGA packages and board-level reliability". 2000. Las Vegas, NV, USA: Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ, USA.

[146] Clech, J.-P.M., et al. "Surface mount assembly failure statistics and failure free time". 1994. Washington, DC, USA: Publ by IEEE, Piscataway, NJ, USA.

[147] Taylor, B.N. and Kuyatt, C.E., *Guidelines for evaluating and expressing the uncertainty of NIST measurement results.*, NIST, Editor. 1994, US Government Printing Office, Washington.

[148] Ghaffarian, R. and Kim, N.P., "Ball grid array reliability assessment for aerospace applications". *Microelectronics Reliability*, 1999. 39(1): p. 107-12.

[149] Xiang, D., et al. "High I/O Glass Ceramic Package PbFree BGA Interconnect Reliability". in *2005 ECTC*. 2005.

[150] Cole, M., et al. "Design and process effects on the reliability of 1.0 mm pitch CBGA". in *SMTA International*. 2000. Rosemont, IL, USA: Surface Mount Technol. Assoc.

[151] Wu, Y.P., Tu, P.L., and Chan, Y.C., "The effect of solder paste volume and reflow ambient atmosphere on reliability of CBGA assemblies". *Transactions of the ASME. Journal of Electronic Packaging*, 2001. 123(3): p. 284-9.

[152] Ries, M.D., et al., "Attachment of solder ball connect (SBC) packages to circuit cards". *IBM Journal of Research and Development*, 1993. 37(5): p. 597-608.

[153] Koschmieder, T., Burnette, T., and Oyler, B. "Ceramic Substrate Thickness, Test Board Thickness, and Part Spacing: a Screening DOE". in *SMTA International.* 1999. San Jose, CA, USA: Surface Mount Tech. Assoc.

[154] Pendse, R., et al. "New CBGA package with improved 2/sup nd/ level reliability". 2000. Las Vegas, NV, USA: IEEE.

[155] Master, R.N. and Ong, O.T. "Ceramic grid array technologies for ACPI applications". 2000. Rosemont, IL, USA: Surface Mount Technol. Assoc.

[156] Ghaffarian, R., "Accelerated thermal cycling and failure mechanisms for BGA and CSP assemblies". *Journal of Electronic Packaging, Transactions of the ASME*, 2000. 122(4): p. 335-340.

[157] Kromann, G.B. "Thermal Management of a C4/ceramic-Ball-Grid Array: The Motorola PowerPC 603 and PowerPC 604 RISC Microprocessors". in *IEEE Semiconductor Thermal Measurement and Management Symposium*. 1996.

[158] Perkins, A. and Sitaraman, S.K. "Acceleration Factor to Relate Thermal Cycles to Power Cycles For Ceramic Area Array Packages". in *SMTA International*. 2005. Chicago, IL: SMTA.

[159] Minitab, *Minitab 13*, Minitab.

[160] Gerke, R.D. and Kromann, G.B., "Solder Joint Reliability of High I/O Ceramic-Ball-Grid Arrays and Ceramic Quad-Flat-Packs in Computer Environments: The PowerPC 603 and PowerPC 604 Microprocessors". *IEEE Transactions on Components and Packaging Technologies*, 1999. 22(4): p. 488.

[161] Master, R.N., et al. "Ceramic Ball Grid Array for AMD K6 Microprocessor Application". in *Electronic Components and Technology Conference*. 1998. Seattle, WA, USA: IEEE, Piscataway, NJ, USA.

[162] Cole, M., et al. "Process optimization for 1.0 mm pitch CBGA". in *SMTA International*. 1999. San Jose, CA, USA: Surface Mount Tech. Assoc.